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A Nullator-Norator Model-Based Approach to Analog Circuit Diagnosis

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Abstract: In the present paper, a model-based nullator-norator approach is developed to automated localization and identification of parametric faults in analog circuits. The *Cadence PSpice* simulator is used for the computer realization of the diagnosis approach. The fault identification is reduced to parametric analysis in the frequency domain of the diagnosis model. An example is presented to demonstrate the feasibility of the proposed approach.

Keywords: Analog circuit diagnosis, fault modeling, model-based diagnosis, parametric faults, nullarors and norators, PSpice simulation.

1 Introduction

THE increasing design complexity and reduced access to analog parts requires the development of efficient diagnosis approaches and tools to test analog and analog-mixed-signal circuits. Several approaches are proposed to automated diagnosis of analog and analog-discrete circuits: model-based approaches, branch decomposition diagnosis at subcircuit and component level, sensitivity-based, symbolic, optimization approaches, etc. [1–7]. Recently, a number of approaches are proposed to investigation of observability of the circuits by optimal test groups determination in order to increase the fault coverage. Model-based approaches are developed for diagnosis of parametric faults [1, 3, 4, 7]. Two basic approaches are applied to the analog circuit diagnosis: using simulation before test (SBT) and using simulation after test (SAT). A SAT diagnosis approach is developed in [7] using

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the program system CLP(R) with the possibility of solving linear set of equations and inequations for localization and identification parametric faults. A model-based approach is proposed in [3] to analog circuit diagnosis, based on parameterized models of the faulty elements. The approach is realized using the possibilities of general-purpose circuit simulators.

In the present paper an approach is developed to automated diagnosis of parametric faults in analog electronic circuits using the circuit simulator *Cadence PSpice* [8, 9]. The isolation of the faulty elements is based on determination of the normalized standard deviations with respect to the predicted mean value of the faulty element parameter. In order to increase the observability, test voltages for a number of test frequencies are used, as well as for different circuit configurations obtained by introducing additional switches in the circuit. A fault prediction approach is applied in order to assess the influence of the design tolerances and to increase the diagnosability of the circuit.

2 Fault Isolation

In order to localize a faulty element, its parameter value is calculated for each of the test frequencies, the mean value $\overline{x}$, as well as variation coefficient V, expressed as by the normalized standard deviation $s/\overline{x}$ [7]. The list of potentially faulty elements is reduced by the elements with negative values and the elements, which are characterized by a large variation coefficients V.

3 Nullor Diagnosis Model

The measured test voltages V_{Ti} of the faulty circuit are applied to the test nodes $i = 1, 2, \ldots, m$ of the diagnosis model using independent voltage source $E_{Ti} = V_{Ti}$ and a nullator (Fig. 1).

By definition, the nullator is characterized by $i = u = 0$ [5]. As a result, the test voltage, corresponding to a faulty circuit, is applied to the test node. In order to test the correctness of a given element, a norator is connected in parallel with the element as shown in Fig. 1. The norator ensures a circuit for the difference current [5], corresponding to the test voltage. The pair nullator-norator (nullor) is equivalent to an ideal operational amplifier. The nullor element (Fig. 2a) can be modeled in the general-purpose circuit simulators using dependent current or voltage source, controlled by voltage or current, with a large controlling coefficient, for example 1×10^9. The *PSpice* realization using VCCS of GVALUE type is presented in Fig. 2b. The parameter definition is shown in Fig. 2c.

As a result of the diagnosis model simulation, the norator current is determined.

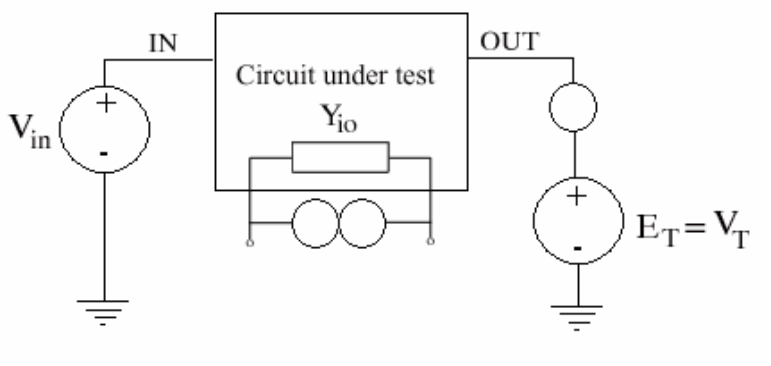
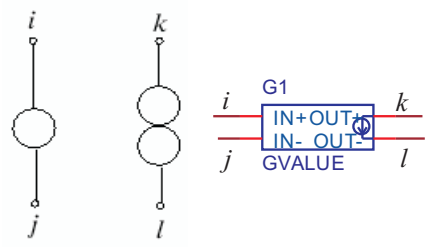


Fig. 1. Nullator-norator diagnosis model of the faulty circuit.



	A
Reference	G_1
Value	GVALUE
EXPR	V(%IN+, %IN-)*1E9

a) b) c)

Fig. 2. Computer model of the nullor: a) nullator-norator pair (nullor); b) PSpice model of the nullor using VCCS; c) parameter definition of VCCS of GVALUE type.

The changed admittance value Y_{id} of the faulty element is determined by the following expression [5]:

$$Y_{id} = Y_{i0} + \frac{I_{ni}}{V_i} \tag{1}$$

where Y_{i0} is the nominal admittance value, I_{ni} is the norator current, V_i is the voltage across the element Y_{i0}, and k is the number of test frequencies.

4 Computer Realization of the Diagnosis Model

The approach to automated diagnosis of analog circuit is illustrated by constructing and investigation of the low-pass filter shown in Fig. 3 [6]. The diagnosis is performed for two test frequencies: 100 Hz and 200 Hz. Let us consider a parametric fault of the capacitor C_1 with a nominal value C_1=100nF and a faulty value C_{1d} =1nF. According to the proposed in [6] DFT methodology, MOS switches are introduced to the individual stages of the filter in order to increase its observability. The filter is tested in different modes of operation: normal mode (all DFT transfor-

mations are disabled - circuit N_1) and individual test mode - a switch is introduced in series with the resistor R_1 and the switch is open (circuit N_2). The measured test voltages for circuits N_1 and N_2 are presented in Table 1.

Table 1. Measured values of the output voltage for the faulty circuit.

Circuit	Frequency[Hz]	Magnitude[V]	Phase[^{o}]
N_1	100	200.39×10^{-3}	176.38
	200	201.57×10^{-3}	172.72
N_2	100	200.79×10^{-3}	180.0
	200	203.21×10^{-3}	180.0

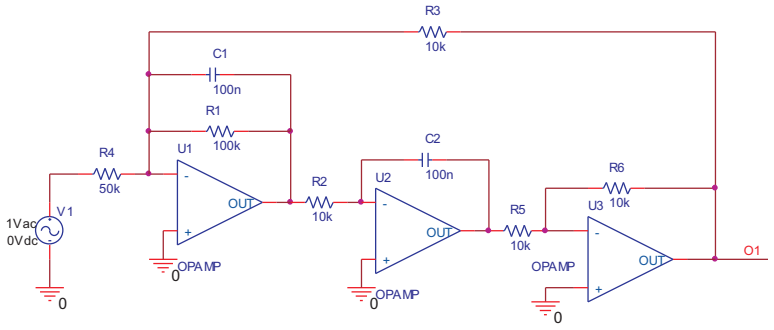


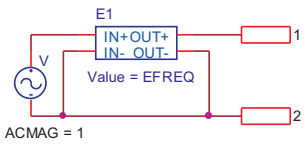
Fig. 3. Low-pass filter.

These values are applied to the test node O_1 using dependent source of VCCS type with parameters defined by a frequency dependent table. It is realized according to the input language of the *PSpice* simulator using the EFREQ element (Fig. 4). The correctness of the possible faulty elements is tested using the connected in parallel norator element. The changed admittance value is calculated form (1).

The parameterized models of the faulty capacitor are shown in Fig. 5a. The subcircuit is defined using parameterized block definition (Fig. 5b). The parameterized model of the faulty resistor is shown in Fig. 6a. The corresponding subcircuit is defined using parameterized block definition (Fig.6b).

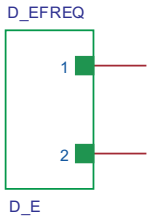
The testing of the faulty elements $q_1, q_2, \ldots, q_n$ is performed using parametric analysis defined by the parameter $par = 1, 2, \ldots, n$. Using the statement IF-THEN-ELSE the VCCS, modeling the norator, is connected in parallel to the corresponding element, when the ID parameter value *num* is equal to its number, otherwise the current of the VCCS is zero:

$$EXPR = V(O1, O2) * IF(PAR == NUM, 1E9, 0).$$



	A
Reference	E_1
Value	EFREQ
magunits	MAG
TABLE	@TAB

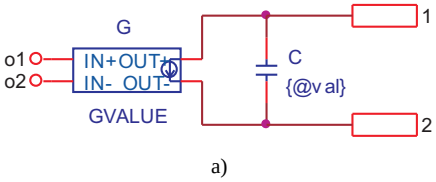
a)



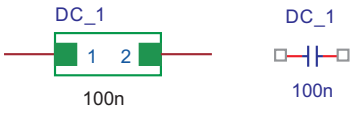
	A
Reference	D_E
Value	D_EFREQ
TAB	(100, 200.394m, 176.385)(200, 201.573m, 172.724)

b)

Fig. 4. Parameterized model for applying the measured voltage to the output node a) subcircuit definition b) block definition.



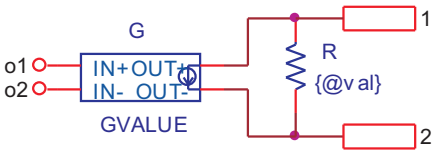
a)



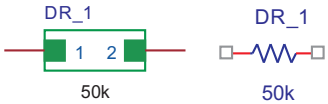
	A
Reference	DC_2
Value	DC
par	{par}
num	2
val	100n

b)

Fig. 5. Parameterized models of the faulty capacitor a) subcircuit definition b) block definition.



a)



	A
Reference	DR_1
Value	DR
par	{par}
num	1
val	50k

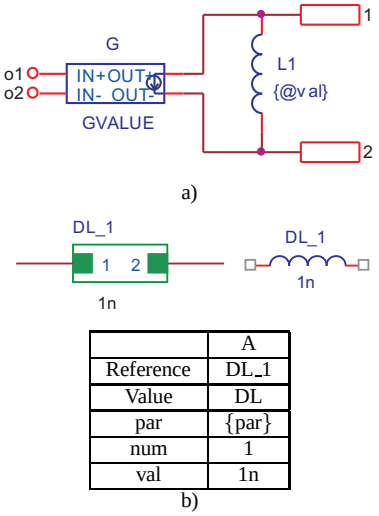
b)

Fig. 6. Parameterized models of the faulty resistor a) subcircuit definition b) block definition.

The parameterized models of the faulty inductor and faulty VCCS are shown in Fig. 7 and Fig. 8 correspondingly.

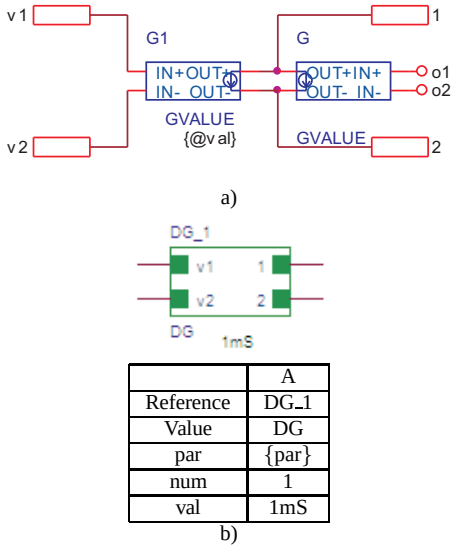
The calculation of the variation coefficient V is performed in the graphical analyzer *Probe*. The determination of the changed resistance values is realized using corresponding macrodefinitions in *Probe* in correspondence with (1) and has the form:

```
R1d =r(V(R1:1,R1:2)/(I(R1)+I(G_R1)))
```



	A
Reference	DL_1
Value	DL
par	{par}
num	1
val	1n

Fig. 7. Parameterized models of the faulty inductor a) subcircuit definition b) block definition.



	A
Reference	DG_1
Value	DG
par	{par}
num	1
val	1mS

Fig. 8. Parameterized models of the faulty VCCS element a) subcircuit definition b) block definition.

Similarly, the capacitances of the faulty capacitors are calculated by the following macrodefinitions:

```
C1d = img((I(C1)+I(G_C1))/V(C1:1,C1:2))/(2*pi*frequency)
```

The mean value *R*1*dmean* from the frequency domain analyses for the test frequencies is:

```
R1dmean = (max(R1d)+min(R1d))/2,
```

and the normalized deviation (variation coefficient V) has the form:

```
R1dn =abs((max(R1d)-R1dmean)/R1dmean).
```

The sum DIST of variation coefficients is calculated for each value of the parameter *par* and the element is selected, corresponding to a minimal value of *par* (Fig. 9). For the considered example DIST has a minimal value for $par = 7$, corresponding to connection of norator in parallel with C_1. Hence, the faulty element C_1 is localized. Using (1), the faulty value $C_{1d} = 0.98$nF is determined. The design tolerances can be taken into account using the fault prediction approach [5]. For this purpose, the difference between test voltages between the successive measurements are applied to the test nodes in order to cancel the influence of design tolerances.

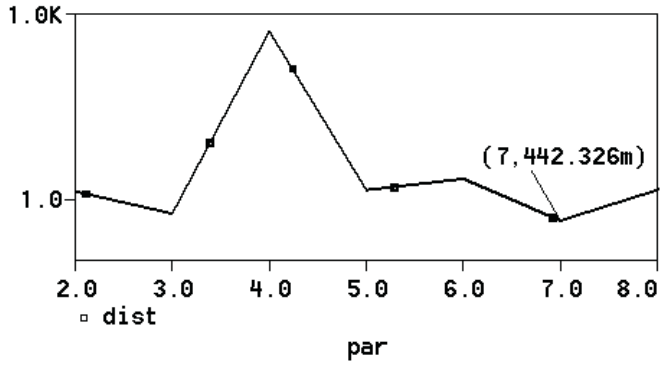


Fig. 9. Determination of the variation coefficient in *Probe*.

5 Conclusions

A model based nullator-norator approach to automated analog circuit diagnosis has been developed in the paper. Parameterized *PSpice* macromodels are built for the faulty elements. The variation coefficient is calculated in the graphical analyzer Probe using corresponding macrodefinitions. The *Cadence PSpice* simulator is used for the computer realization of the diagnosis approach. The fault identification is reduced to parametric analysis in the frequency domain of the diagnosis nullator-norator model. The isolation of the faulty elements is based on determination of normalized standard deviations from the predicted mean parameter value of the faulty element. In order to increase the fault observability, the results for the test voltages at different frequency points are used. Parameterized models of the faulty components are proposed based on IF-THEN-ELSE description. An example is presented to demonstrate the feasibility of the proposed approach.

Acknowledgements

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