Quaternary Regenerative CMOS Logic Circuits With High-Impedance Output State

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Abstract: Principles and possibilities of synthesis and design of quaternary multiple-valued regenerative CMOS logic circuits with high-impedance output state are described and proposed in the paper. Two principles of synthesis and implementation of CMOS regenerative quaternary multiple-valued logic circuits with high-impedance output state are proposed and described: the simple circuits with smaller number of transistors, and the buffer/driver circuits with decreased propagation delay time. The schemes of such logic circuits are given and analyzed by computer simulations. Some of computer simulation results confirming descriptions and conclusions are also given in the paper.

Keywords: Quaternary multiple-valued logic circuits, regenerative logic circuits, high-impedance output state, CMOS logic circuits, computer simulation, pSpice simulation.

1 Introduction

Digital systems that are practically in use are still binary digital systems. However, with rapid development of LSI and VLSI technologies, the possibilities and reasons for implementation of digital systems with the logic basis greater than 2 (multiple-valued or MV systems and logic) are becoming real and applicable [1]-[4].

Advantages and good characteristics of MV logic systems and circuits are created great interest for practical design and implementation of such systems and

circuits [1]-[4]. There are many advantages of MV logic systems and circuits comparing with the binary ones. The main advantages of MV logic are: greater speed of arithmetic operations, greater density of memorized information, better usage of transmission paths, decreasing of interconnections complexity and interconnections area, decreasing of pin number of integrated circuits and printed boards, possibilities for easier testing of digital systems [1, 2].

Practically, the greatest interest is for and the most investigated, developed and implemented are the ternary (with the logic basis of 3) and quaternary (with the logic basis of 4) MV circuits and systems [1]-[4]. The first investigated and practically implemented have been ternary MV circuits and systems. Later, the greatest practical interest exists for investigation and application of quaternary logic systems and circuits.

The common buses are mainly used method for the data transmission in the binary digital systems. Connection to the buses is implemented by the logic circuits with high-impedance output state. Because of the same reasons as in the binary systems, the common buses and the logic circuits with high-impedance output state are also used in the multiple-valued digital systems [1, 2]. Of course, also exists the need for noise influence decreasing in such MV digital circuits and systems. So, there is need for using regenerative MV circuits with high-impedance output state.

The reasons and advantages for application of CMOS technology in implementation of binary digital systems and circuits are very well known. All these good characteristics should be also kept in MV logic systems and circuits. There are also some advantages of CMOS technology that are important and characteristic for MV logic [1]-[4]. Also, since the first papers about MV logic circuits implementation, the greatest interest exists for implementation in CMOS technology.

Possibilities and methods of synthesis and design of quaternary regenerative CMOS logic circuits with high-impedance output state are considered in the paper. Methods for synthesis and design of such CMOS MV logic circuits are proposed and detailed described. Two principles of synthesis and implementation of quaternary regenerative CMOS MV logic circuits with high-impedance output state are proposed and described: the simple circuits with smaller number of transistors, and the buffer/driver circuits with decreased propagation delay time. The concrete schemes of such bus interface quaternary regenerative CMOS logic circuits with high-impedance output state are given and analyzed by computer simulations. All proposed principles and results have been analyzed and confirmed by PSPICE simulation for one CMOS technology process [5]. Some of computer simulation results confirming descriptions and conclusions are also given in the paper.

2   Design Of Quaternary Regenerative CMOS Logic Circuits With High-Impedance Output State

There are two methods to obtain high-impedance output state in the CMOS quaternary logic circuits: using CMOS transmission gate at the circuit output, or disconnecting the circuit output from the supply voltages. The possibilities and concrete realizations of CMOS quaternary circuits with high-impedance output state are proposed and described in paper [6]. Methods for obtaining and design of regenerative quaternary CMOS logic circuits are considered, given and described in paper [7].

Two types of CMOS quaternary regenerative circuits with high-impedance output state are considered, proposed and described here: the simple circuits with minimal number of transistors and the buffer/driver circuits with powerful output and decreased propagation delay time.

2.1   Simple Circuits

The principle schemes of simple CMOS quaternary regenerative circuits with high-impedance output state are shown in Fig. 1.
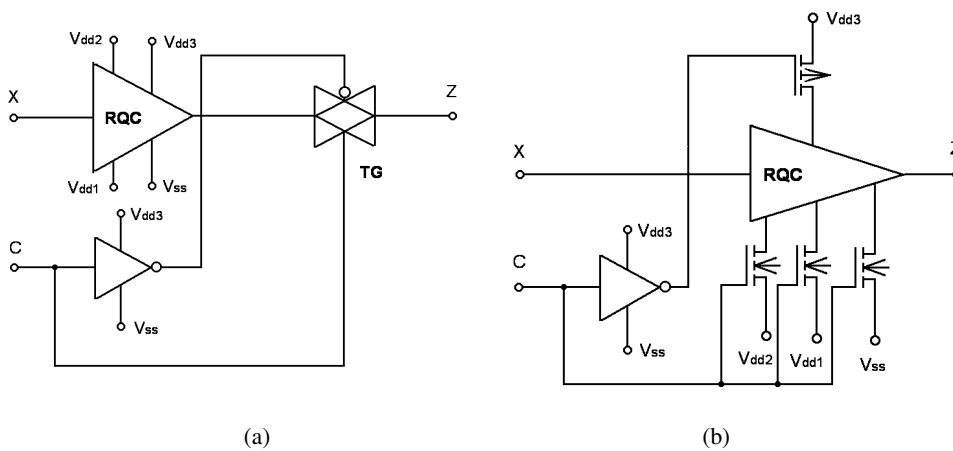

(a)   (b)

Fig. 1. Principle schemes of simple circuits realization.

The circuit in Fig. 1(a) has the CMOS transmission gate (TG) at the output of regenerative CMOS quaternary circuit (RQC). Standard CMOS inverter is used for control of CMOS transmission gate. For C=3 transistors in transmission gate are turned on and then is $Z = X$. In that case there is voltage histeresys in static voltage transfer characteristic of the circuit. So, it exists a greater noise immunity of the circuit. For C=0 transmission gate is off and the output of the circuit is in the high-impedance state.

The circuit in Fig. 1(b) has additional transistors connected between regenerative CMOS quaternary logic circuit (RQC) and the supply voltages. These serial transistors disconnect the circuit output from supply voltages in the high-impedance state. For C=3 all additional transistors are turned on and then is $Z = X$. In that case there is greater noise immunity of the circuit. For $C = 0$ all additional transistors are turned off and the circuit output is in the high-impedance state.

Schemes of the simple circuits with minimal number of transistors, obtained on the principles shown in Fig. 1., are proposed and given in Fig. 2. These circuits use the regenerative quaternary CMOS identity circuit [7] at the input. Circuit in Fig. 2(a) has standard CMOS transmission gate at the output that is turned on for C=3 and turned off for C=0. Circuit in Fig. 2(b) has serial connection of MOS transistors at the output of regenerative quaternary CMOS identity circuit. This enables obtaining of high- impedance at the output for $C = 0$ when two of serially connected MOS transistors are turned off. The input regenerative quaternary CMOS identity circuits are obtained according to principles given in paper [7]. According to paper [7], binary regenerative CMOS logic circuits are used at the input of circuits in Fig. 2(a) and Fig. 2(b). Binary regenerative CMOS circuits that are used here are proposed and described in paper [8]. Standard binary CMOS inverters in feedback loop give voltage histeresys in voltage transfer characteristic of the circuits.

(a)   (b)
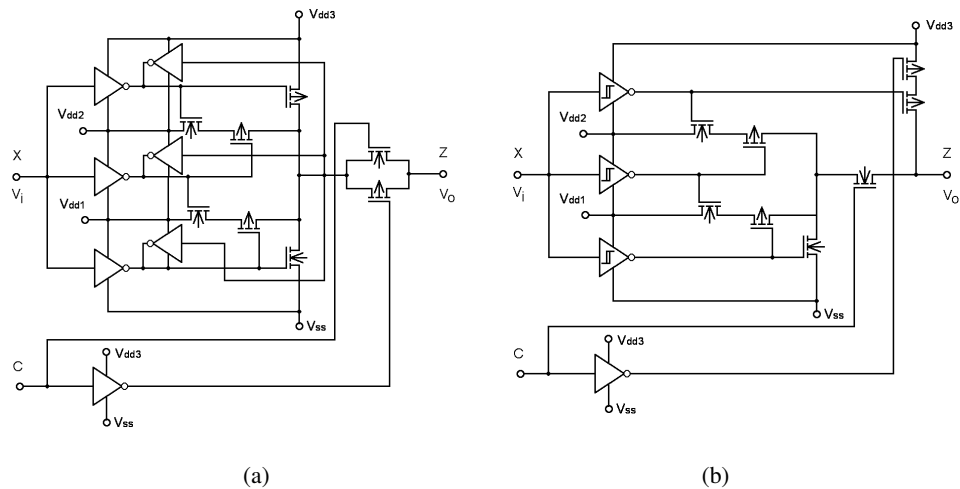
Fig. 2. Schemes of simple circuits realization.

Good characteristics of the simple circuits are minimal number of transistors and small propagation delay times when capacitive load of the circuit is small. The disadvantage is serial connection of output MOS transistors, what produces great propagation delay times when capacitive load of the circuit is greater.

Characteristics of the simple circuits from Fig. 2 have been analyzed by PSPICE simulation. Some results of the PSPICE simulation of circuits from Fig. 2 are given in Fig. 3 and Fig. 4. The static voltage transfer characteristics of both circuits for $C = 3$ are very similar. The characteristic obtained by simulation is shown in Fig. 3. The threshold voltages of the circuit can be obtained in the same way as for quaternary regenerative CMOS circuits or for binary CMOS regenerative circuits [7, 8]. It can be shown that the threshold voltages of the circuit are given by

$$V_{th1} = \frac{1}{2}(V_{dd} + V_{h1}), \tag{1}$$

$$V_{tl1} = \frac{1}{2}(V_{dd} - V_{h1}), \tag{2}$$

$$V_{th2} = \frac{1}{2}(2V_{dd} + V_{h1}), \tag{3}$$

$$V_{tl2} = \frac{1}{2}(2V_{dd} - V_{h1}), \tag{4}$$

$$V_{th3} = \frac{1}{2}(3V_{dd} + V_{h1}), \tag{5}$$

$$V_{tl3} = \frac{1}{2}(3V_{dd} - V_{h1}). \tag{6}$$

The voltage histeresis for any of change of input voltage are given by

$$V_{h1} = V_{h2} = V_{h3} = \frac{V_{dd}(3V_{dd} - 4V_{th})}{4k(V_{dd} - 2V_{th}}. \tag{7}$$

In the given equations coefficient k is ratio of MOS transistors transconductances. Coefficient k is here given by ratio of transconductanse of input MOS transistors, and transconductanse of MOS transistors in feedback loop. With V_{tn} are marked threshold voltages of MOS transistors.

Results of dynamic characteristics simulation for circuit from Fig. 2(a) are given in Fig. 4. Average propagation delay time as a function of C_L is shown in Fig4a. Average propagation delay times for the transition of circuit output to and from high-impedance state as a function of C_L are shown in Fig. 4(b). In Fig. 7(b) t_{dSH} is average delay time of transition from some of static states to high-impedance state, and t_{dHS} is average delay time for transition from high-impedance state to some of static states. Given results in Fig. 3 and Fig. 4 have been obtained by simulation for $R_L = 50\text{k}\Omega$, for supply voltages $V_{SS} = 0\text{V}$, $V_{dd1} = 3\text{V}$, $V_{dd2} = 6\text{V}$, $V_{dd3} = 9\text{V}$ when the circuits are symmetrical and for one CMOS technology process [5].
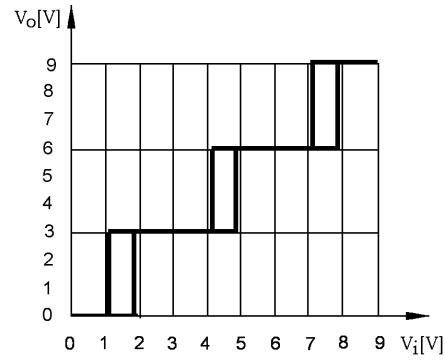
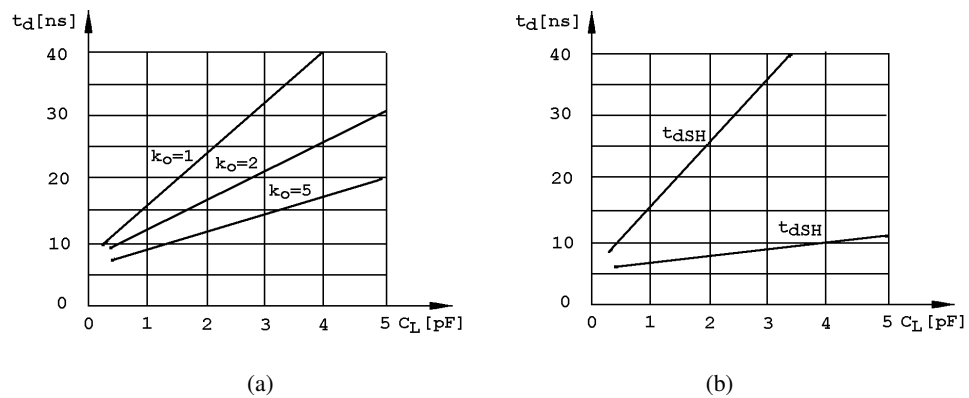Fig. 3. Static voltage transfer characteristic of circuits in Fig.2.

(a)   (b)

Fig. 4. Dynamic characteristics of circuit in Fig. 2(a).

2.2   Buffer/Driver Circuits

Buffer/driver circuits should use schemes with minimal number of CMOS output transistors. The principle scheme for synthesis of CMOS regenerative quaternary buffer/driver circuits with high-impedance output state is proposed here and is shown in Fig. 5. The output part of the circuit is similar as in standard CMOS quaternary circuits. Appropriate CMOS control logic is used for control of circuit output transistors. This control logic turns on or turns off the output CMOS transistors depending on logic state at information input X and control input C and gives histeresys in static voltage transfer characteristic of the circuit. For $C = 3$ the circuit works as the standard CMOS regenerative quaternary circuit and then is $Z = X$ and exists voltage histeresys. For $C = 0$ the output of the circuit is in high-impedance state. Needed output power is obtained by adequate design of output CMOS transistors only.
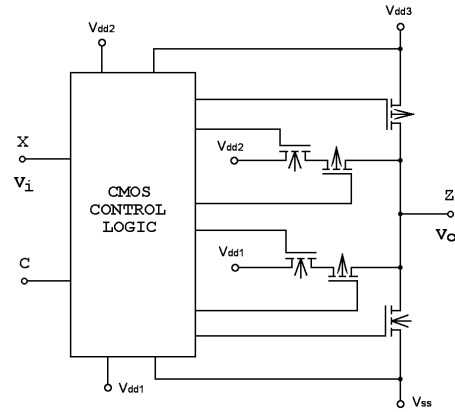
Fig. 5. Principle scheme of regenerative buffer/driver circuit.

It is possible to obtain different schemes of CMOS regenerative quaternary buffer/driver circuits on the basis of principle from Fig. 5. Difference between the solutions is in the way of realization of CMOS control logic. One solution, the circuit with control logic realized by binary regenerative CMOS NAND and NOR circuits and standard binary CMOS inverters is shown in Fig. 6. The binary regenerative CMOS NAND and NOR circuits give histeresys and greater noise immunity for the circuit.
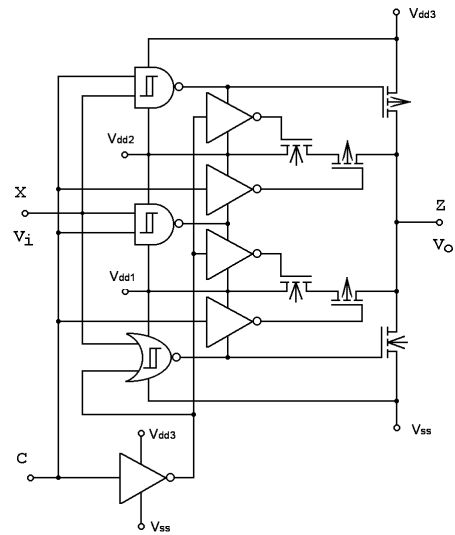
Fig. 6. One possibility of realization of buffer/driver circuits.

However, the optimal buffer/driver CMOS quaternary regenerative high-impedance circuit both by number of transistors and by working speed is shown in Fig.7. This circuit uses CMOS transistors network as the control logic for output transistors. MOS transistors in feedback loop give histeresys in voltage transfer characteristic and increased noise immunity of the circuit.

Characteristics of the regenerative buffer/driver circuits have also been analyzed by PSPICE simulations. Some results of the simulation of optimal buffer/driver circuit from Fig. 7 are given in Fig. 8. The static voltage transfer characteristic for $C = 3$ is very similar to the characteristic given in Fig. 3. The threshold voltages of the circuit can be obtained in the same way as for quaternary regenerative CMOS circuits or for binary CMOS regenerative circuits [7, 8]. Here given equations (1) to (7) can be used for calculation of threshold voltages. So, the dynamic characteristics are only shown here. Average propagation delay time as a function of C_L is shown in Fig. 8(a). Average propagation delay times for the transition of circuit output to and from high-impedance state as a function of C_L are shown in Fig.8b. Given results have been obtained for the same conditions as the results for circuits in Fig. 2 that are shown in Fig. 3 and Fig. 4.
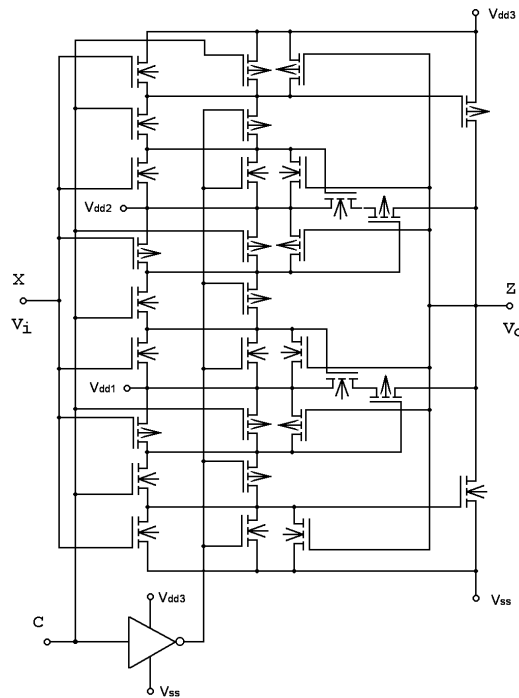

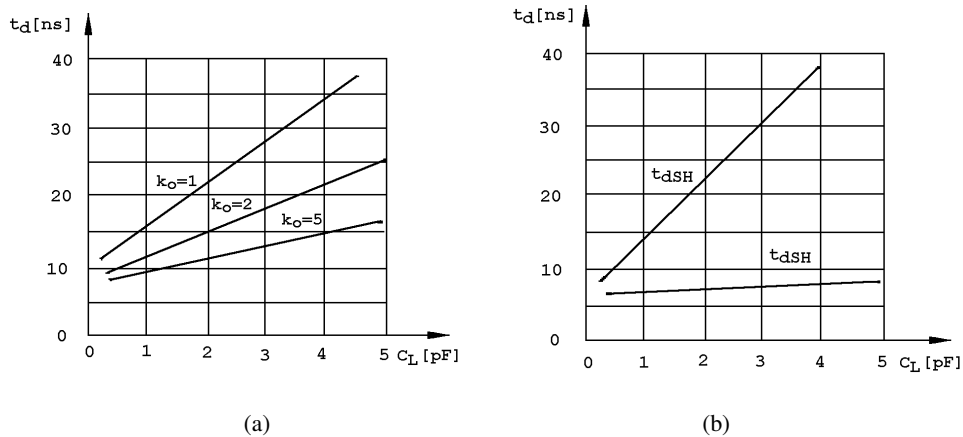Fig. 7. Scheme of optimal regenerative buffer/driver circuit.

Fig. 8. Dynamic characteristics of buffer/driver circuit in Fig.7.

The regenerative buffer/driver circuits are more complex, with more transistors, than the simple regenerative circuits. But, the buffer/driver circuits have greater output power and smaller propagation delay times when driving lines with heavy capacitive loads as the common bus lines are.

3 Conclusions

Here proposed principles and solutions give possibility to obtain and design regenerative quaternary CMOS circuits with high-impedance output state. These circuits are fully CMOS circuits, without static power consumption. The circuits can be easily synthesized and designed according to working conditions of the circuit.

Two types of proposed regenerative quaternary CMOS circuits with high-impedance output state are described. The simple circuits, comparing with the buffer/driver ones, have less number of transistors. But, these circuits have greater propagation delay time for greater capacitive loads, and the circuit area increases much more when the output driving capability increases. So, the simple circuits need to be used inside of LSI and VLSI circuits, at smaller working frequencies and small capacitive loads, in situations when the most important is to obtain high-impedance state and increased noise immunity. The buffer/driver circuits have to be used at greater working frequencies and greater capacitive loads.

The buffer/driver circuits can be used as input or output circuits of LSI and VLSI systems, or as integrated circuits of smaller scale of integration for connection to quaternary buses (separated bus interface circuits).

References

[1] D. C. Rine, *Computer science and multiple-valued logic: theory and applications.* Amsterdam: North-Holland Publishing Company, 1984.

[2] K. C. Smith, "Multiple-valued logic: a tutorial and appreciation," *Computer*, pp. 17–27, Apr. 1988.

[3] A. K. Jain *et al.*, "CMOS multiple-valued logic design-part I, part II," *IEEE Trans. on CAS-I: Fundamental theory and applications*, pp. 505–522, Aug. 1993.

[4] N. R. Shanbhag *et al.*, "Quaternary logic circuits in 2μm CMOS technology," *IEEE Journal of Solid State Circuits*, pp. 790–799, June 1990.

[5] C. H. Diaz *et al.*, "An accurate analytical delay model for BiCMOS driver circuits," *IEEE Trans. on Computer- Aided Design*, no. 5, pp. 577–588, 1991.

[6] D. Bundalo, B. Đorđević, and Z. Bundalo, "Bus interface circuits in quaternary digital electronic systems," in *Proc. of Inter. Scientific Conference UNITECH'02*, Gabrovo, Bulgaria, 2002, pp. 87–91.

[7] Z. Bundalo and D. Bundalo, "Regenerative quaternary CMOS logic circuits," in *Proc. of 4th Conference of INDEL*, Banja Luka, Republic of Srpska, Bosnia and Herzegovina, 2002, pp. 56–60, (in Serbian).

[8] Z. Bundalo and B. Dokić, "Non-inverting regenerative CMOS logic circuits," *Microelectronics Journal*, vol. 16, no. 5, pp. 7–17, 1985.