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Design of Quaternary Logic Systems and Circuits

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Abstract: The principles and possibilities of design of fully quaternary multiple valued combinational logic systems and circuits are described and proposed in the paper. Different ways of design of fully quaternary combinational logic systems and circuits are considered and described first. Then algorithm for automated computerized design of such systems and circuits is considered and proposed. The algorithm gives possibility for synthesis and optimization of quaternary logic systems and circuits. It is applied on design of CMOS quaternary multiple valued logic systems and circuits. The algorithm includes the most important aspects of design of quaternary logic circuits: logic circuit scheme synthesis and logic circuit optimization. Methods for synthesis of quaternary CMOS combinational logic circuits are proposed and described. Also, method for optimization of CMOS quaternary logic circuits, according to operation conditions and needed characteristics, is proposed and described. Design procedure is realized by personal computer using PSPICE for circuit simulation. Computer PSPICE simulation results confirming described methods and conclusions are given in the paper.

Keywords: Multiple valued logic systems and circuits, quaternary logic systems and circuits, automatization, combinational logic systems and circuits, CMOS logic circuits, circuit synthesis, circuit optimization, computer simulation.

1 Introduction

Good characteristics and advantages of multiple-valued (MV) digital electronic (logic) systems and circuits are created great interest for its practical implementation [1]-[4]. There are many advantages of such logic systems and circuits comparing with the binary ones. The main advantages of MV logic systems and circuits

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are: greater speed of arithmetic operations realization, greater density of memorized information, better usage of transmission paths, decreasing of interconnections complexity and interconnections area, decreasing of pin number of integrated circuits and printed boards, possibilities for easier testing [1]-[4].

Although in practice still there are not many fully multiple valued digital systems, some parts of a binary digital system are often realized using MV logic [1, 2]. The greatest practical interest is for application of quaternary (where the basis is 4) multiple valued logic systems and circuits and for implementation in CMOS technology [1]-[4]. Good characteristics of CMOS technology in binary logic systems and circuits are the reasons that the CMOS technology is the most often used also for design and implementation of quaternary circuits and systems.

The principles and possibilities of design of fully quaternary multiple valued combinational logic systems and circuits are described and proposed in the paper. Different ways of design of fully quaternary combinational logic systems and circuits are considered, proposed and described first. Then algorithm for automated computerized design of such systems and circuits is considered and proposed. The algorithm gives possibility for synthesis and optimization of fully quaternary logic systems and circuits. It is applied on design of CMOS quaternary multiple valued logic systems and circuits. The algorithm includes the most important aspects of synthesis and optimization of quaternary logic circuits: logic circuit scheme synthesis and logic circuit optimization. Methods for synthesis of quaternary CMOS logic circuits are proposed and described. Also, method for optimization of CMOS quaternary logic circuits, according to operation conditions and needed characteristics, is proposed and described. Design procedure is realized by personal computer using PSPICE for circuit simulation. Computer PSPICE simulation results confirming described methods and conclusions are given in the paper. All proposed principles and circuits and given results have been analyzed and confirmed by PSPICE simulation for one CMOS technology process

2 Design of Quaternary Logic Systems

Practically, there are two standard architectures and methods for design of multiple valued digital and computer systems: so called fully MV systems and mixed MV systems [1, 2]. Fully multiple valued systems use only MV logic circuits with the same MV logic basis. Mixed MV systems use combination of MV logic circuits and standard binary logic circuits, where a part of the system is realized by using binary logic circuits. Also, very often MV logic is used for realization of some functions inside of binary digital systems [1, 2].

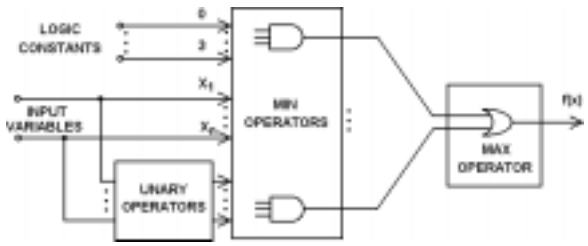
Practically, there are two standard methods for design of MV logic circuits and systems: so called fully MV systems and mixed systems [1]-[3]. So, quaternary logic circuits and systems can also be fully quaternary systems and mixed systems. Fully quaternary systems use only quaternary logic circuits with the same logic basis. Mixed quaternary systems use combination of quaternary logic circuits and standard binary logic circuits, where a part of the system is realized by using binary logic circuits. Also, very often quaternary logic is used for realization of some functions inside of binary digital systems [1, 2]. The fully quaternary combinational logic systems and circuits will be considered here only.

The fully multiple valued logic systems, as well as binary systems, can be designed by more ways and can have different possible structures, mainly depending on basic logic components used. Such systems can be realized by using max, min and unary operators (circuits), using operators of sum by module and product by module type, using T operators, using multithreshold operators. There are also other methods of design and architectures of such digital systems, based on using MV spectral techniques, using strongly structured realizations (structures of ROM and PLD type) and using iterative cell matrixes [1, 2].

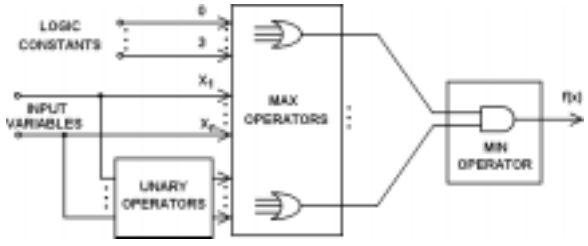
The first method, with using of quaternary max, min and unary operators, is the most frequently used. The two principal designs of quaternary logic circuit or network with using quaternary max, min and unary operators are shown in Fig.1. These circuits realize quaternary MV logic function of sum of products type. These are designs of combinational logic circuits and systems. All the min, max and unary circuits in Fig.1 are quaternary logic circuits. Also, all input variables and output variable are quaternary variables. Quaternary CMOS min (AND) and max (OR) type logic circuits are proposed and described in paper [5]. Those logic circuits can be used for realization of CMOS quaternary logic network and circuit with any quaternary logic output function.

Methods and procedures for design of standard quaternary networks and systems are very similar to ones used in binary systems [1]-[3]. Quaternary logic systems in practice are designed using same methods and procedures as for design of binary systems. The design has a sequence of steps, iterations and interactions. The objective of these activities is, starting from functional requirements of the system, to obtain the system design that can be practically realized as easy as possible. This procedure is realized at more levels of presentation of the system. As well as in binary system, the solution is represented at three levels: logic level, functional level and algorithmic level. Also, at every of solution presentation levels there are three basic activities: synthesis, optimization and analysis.

Here it will be considered first two activities in design of quaternary CMOS logic systems and circuits: synthesis and optimization. It will be proposed and



(a)



(b)

Fig. 1. Principles of design of quaternary logic network or circuit using max, min and unary circuits.

described method of synthesis and optimization of fully quaternary CMOS system or circuit. For analysis it is used PSPICE simulation.

3 Synthesis of Quaternary CMOS Logic Systems and Circuits

Synthesis of quaternary logic systems and circuits, as well as in binary systems and circuits, is realized as a synthesis of logic cells that are used in the system. All the system is decomposed in quaternary logic cells and synthesis is performed for each of specific quaternary cells. This procedure is still mainly interactive and dependent on experience and skill of designer. In the process first are defined all possible electrical schemes for a certain type of quaternary logic cell. This is realized by designer before the design process for all possible quaternary logic cells that will be used in the system. Then the selection of electrical scheme for each concrete quaternary logic cell is performed. If there are more possible schemes for some type of quaternary logic cell then it is performed selection of the scheme that will be optimal at concrete place in the system according to concrete working conditions. That procedure is mainly completely automatised.

Standard procedure for synthesis of quaternary CMOS logic systems and circuits is similar as for binary CMOS logic systems synthesis. It is synthesis of the logic network using standard CMOS quaternary logic circuits or cells. The most

frequently used standard quaternary logic circuits for the synthesis are max, min and unary circuits (Fig.1.). The standard CMOS quaternary logic circuits, i. e. quaternary CMOS logic cells, should be adequately synthesized and implemented [5]. All this is complicated and it is very complicated to obtain optimal design.

One simple principle for synthesis of CMOS quaternary logic circuits and systems is proposed and described here. It enables application of methods and procedures used for synthesis of standard binary CMOS logic circuits and systems. This principle does not use standard CMOS quaternary logic circuits as in Fig.1. It uses standard CMOS binary logic circuits and appropriate quaternary CMOS output stage [6]. Such, we obtain more simple procedure for synthesis as well as more simple solutions. The proposed method for the synthesis is shown in Fig. 2.

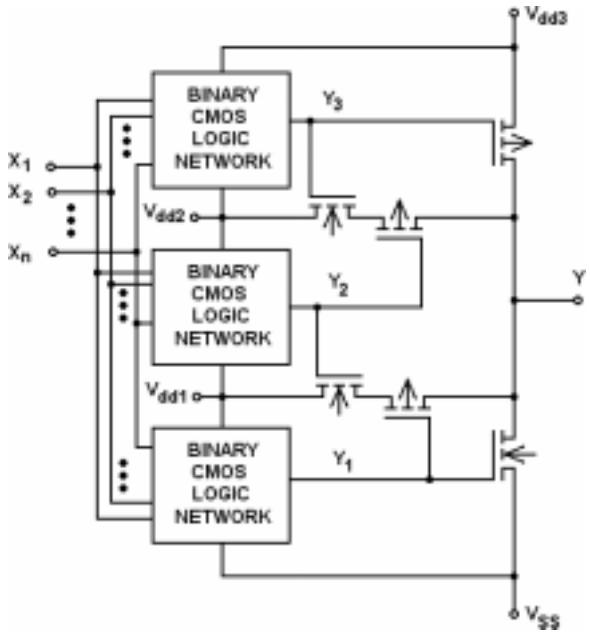


Fig. 2. Proposed method for design and synthesis of quaternary CMOS logic circuits.

Synthesis of input binary logic circuits can be realized in a different ways, first of all depending on used basic binary CMOS circuits. So it can be more different concrete solutions of all MV logic circuit or cell. Next phase in the design is selection of most appropriate solution for concrete working conditions in MV system.

As it can be seen in Fig.2, the proposed method uses three identical binary standard CMOS logic networks at the input, conected beetwen diferent supplay voltages, and apropriate quaternary CMOS output stage. The three input binary

CMOS networks define the logic function of whole quaternary circuit. The CMOS quaternary output stage is controled by the three binary CMOS networks and is giving four output states.

The three binary CMOS logic networks at the input are realizing the same binary logic function. That binary function is inverse function of the quaternary output circuit function, i. e. binary function is given by

$$Y_1 = Y_2 = Y_3 = \overline{Y} = \overline{f(X_1, X_2, \ldots, X_n)}, \tag{1}$$

where Y or $f(X_1, X_2, \ldots, X_n)$ is the output function that should be realized by the quaternary circuit.

So, this proposed principle of synthesis of CMOS quaternary logic circuit or network is based on synthesis of binary CMOS logic networks with binary logic function given by equation (1). Such, we obtain needed quaternary logic function of realized quaternary circuit or network. CMOS output stage from Fig. 2 gives four quaternary output levels of whole quaternary circuit or network.

Synthesis of input binary logic circuits can be realized in a different ways, first of all depending on used basic binary CMOS circuits. So it can be more different concrete solutions of all quaternary logic circuit or cell. Next phase in the design is obtaining of most appropriate solution for concrete working conditions in quaternary system.

Two procedures of the synthesis are proposed here: basic principle and improved principle. The principles will be shown here on the example of synthesis of quaternary circuit with quaternary logic function given by

$$Y = f(X_1, X_2, X_3) = X_1X_2 + X_1X_3. \tag{2}$$

So, it is necessary to realize three CMOS binary networks with binary function given by

$$Y_1 = Y_2 = Y_3 = \overline{Y} = \overline{X_1X_2 + X_1X_3} = \overline{X_1(X_2 + X_3)}. \tag{3}$$

3.1 Basic principle of synthesis

The basic principle of synthesis proposed here is very simple. The three binary CMOS logic networks at the input of quaternary circuit are realized using standard CMOS binary logic circuits. So, the same methods as for synthesis of binary logic circuits are used here for synthesis of quaternary logic circuits. That is the advantage of this principle of synthesis.

There are possibilities to obtain different binary CMOS logic networks for the same binary logic function, depending of the basic binary circuits used and methods

used for optimization of scheme of binary logic network. In the synthesis it is needed and necessary to use all methods for minimization used in binary digital systems synthesis. In Fig.3 it is given one possible synthesis of the quaternary circuit with logic function given by equation (2). It is used relation (3) for synthesis where it was made transformation of original binary function in equation (2). If it is used other possibility for transformation and minimization of binary function given by equation (2) then it could be obtained other form of the same function and other form of design of the quaternary circuit. It can be concluded that the circuit in Fig.3 is simple and simpler then the solution that can be obtained by design in Fig.1. It uses less number of transistors and has less average propagation delay time than the solution obtained by design in Fig.1. The conclusion about less average propagation delay time has been verified by PSPICE simulation.

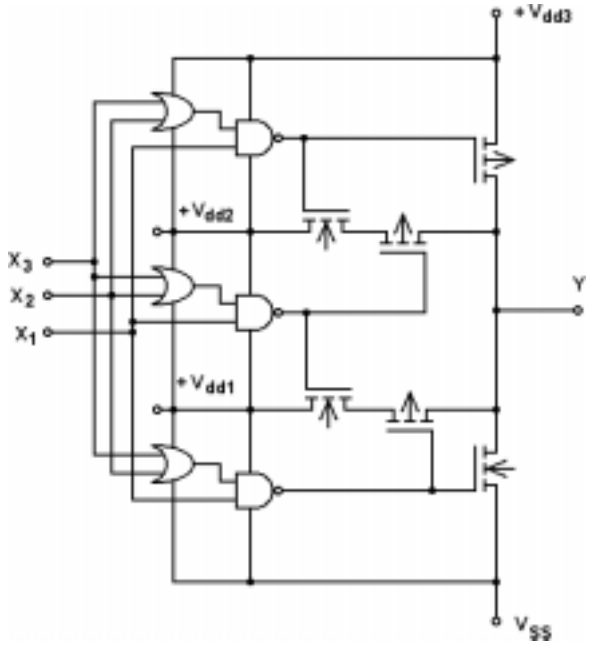


Fig. 3. Design of quaternary CMOS circuit with logic function given by equation (2).

3.2 Improved principle of synthesis

In the improved principle of synthesis the binary CMOS logic networks at the input of quaternary circuit are realized as the matrixes of standard CMOS transistors. This principle of design reduces the total number of used MOS transistors and number of stages in input binary CMOS networks. So, the total circuit area of the

quaternary CMOS circuit is reduced and the working speed is increased comparing with basic principle of synthesis.

The practical way of synthesis of quaternary CMOS logic circuit with output logic function given by equation (2) is shown in Fig.2. It is very easy to realize necessary binary logic function given by equation (3) using matrix of CMOS transistors. The same methods used for synthesis of standard binary CMOS logic circuits with more complex output function are also used here. Adequate matrix of CMOS transistors should be synthesized and designed. The output stage is the same as in proposed scheme in Fig.2.

The complete scheme of quaternary CMOS logic circuit with output quaternary function given by equation (2) is shown in Fig.4. It can be seen from Fig. 4 that all three input CMOS binary networks are the same, connected between four different supply voltages. The input binary networks adequately control the CMOS output stage, such producing four CMOS output quaternary levels. The total circuit area of the quaternary CMOS circuit in Fig.4 is reduced and the working speed is increased comparing with basic principle of synthesis and circuit in Fig.3. The conclusion about smaller average propagation delay time has been confirmed by PSPICE simulation.

4 Optimization of Quaternary CMOS Logic Circuits

Next step after synthesis is optimization of quaternary CMOS logic circuit or network. The standard procedure of optimization, as for binary logic circuits, consists of two steps: optimization of each logic circuit (i. e. logic cell) separately and optimization of whole logic network.

Optimization of quaternary logic systems and circuits, as well as in binary systems and circuits, is in essence optimization of quaternary logic cells or circuits that are previously synthesized and that form quaternary system. Each quaternary logic cell is optimized separately depending of working place and working conditions of the cell in quaternary system. Working conditions for each logic cell are known: average propagation delay time, fan-out factor, noise immunity, supply voltages. Optimization of quaternary logic cell is optimization of cell area with aim to obtain minimal cell area and satisfying working conditions. That optimization procedure depends on used technology process and used quaternary logic cell. That procedure can be also completely automatized.

The method for optimization of the proposed CMOS quaternary logic circuits or cells is also proposed and described here. It consists of two procedures: optimization of binary CMOS logic networks at input of quaternary circuit and opti-

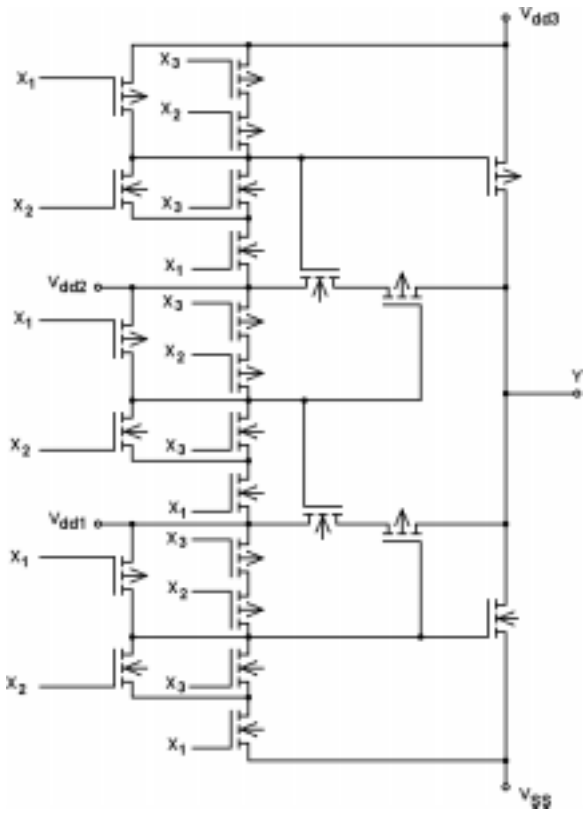


Fig. 4. Design of quaternary CMOS circuit using CMOS transistors matrix for function given by equation (2).

mization of quaternary CMOS output stage.

4.1 Optimization of input CMOS binary networks

The optimization of binary CMOS networks at input of quaternary circuit can be realized in a similar way as for optimization of CMOS binary circuits since here are used binary CMOS circuits. Here it can be used same principles as for binary CMOS logic circuits. Optimization is performed according to circuit working characteristics and conditions. Here it means that it should determine ratio K of PMOS and NMOS transistor channel width to obtain minimum circuit area and appropriate circuit characteristics. Here proposed criteria is given by

$$F = \frac{t_{da}\Delta t_d}{NI_R} \tag{4}$$

where t_{da} is average propagation delay time, Δt_d is absolute difference of edge delays of output signal, NI_R is noise immunity referring to supply voltage. It should minimize value F as a function of ratio K. The ratio K with minimal F is value of K that should be applied in the circuit. Criteria F as a function of ratio K should be obtained by computer simulation.

Dependence of criteria F on ratio K for quaternary CMOS circuit from Fig.4, obtained by PSPICE simulation, is shown in Fig.5. From the dependence it should be selected ratio K for what criteria F has minimal value.

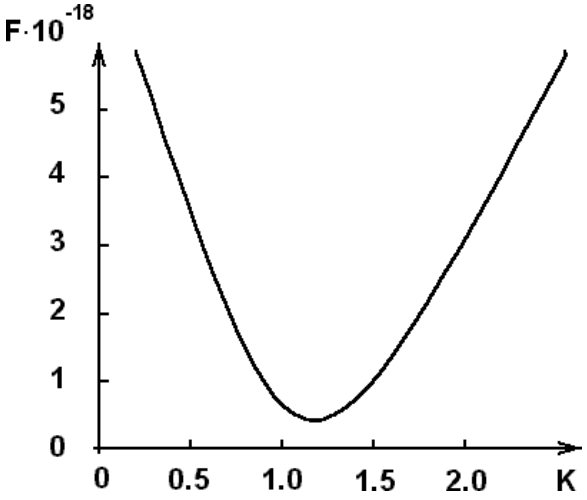


Fig. 5. Criteria F as a function of ratio K for quaternary CMOS circuit in Fig.4.

4.2 Optimization of CMOS quaternary output stage

The task of optimization of CMOS quaternary circuit output stage is to determine channel widths of output PMOS and NMOS transistors. Optimization is performed according to working conditions of the quaternary circuit: maximally allowed average propagation delay time, fan-out factor, and supply voltage.

The optimization should determine minimal value of ratio $k_o = W_o/W_S$, where W_o is output MOS transistor channel width and W_S is standard MOS transistor channel width. For real fan-out factor M_r and maximally allowed average propagation delay time t_{dar}, approximately can be determined k_o. The way of this optimization is principally shown in Fig.6. The average propagation delay time (t_{da}) as a function of k_o for fan out factor $M_r = 6$, obtained by PSPICE simulation, is shown in Fig.6.

The procedure of optimization is as follows. First, it should be determined by computer simulation dependence of t_{da} on k_o for known fan-out factor M_r of the CMOS quaternary circuit. That dependence is shown in Fig.6. Then, it can be determined from the dependence the real ratio k_{or} what is necessary for the real allowed average propagation delay time t_{dar} of the quaternary circuit. Then it should be selected the closest greater possible value of ratio k_o as a value of k_o that will be practically used. To make the procedure shorter and quicker it is enough to perform circuit simulation only for real fan-out factor M_r and for different values of ratio k_o until it will be obtained the first possible k_o value for what it will be t_{da} less than t_{dar}. It has been illustrated by dashed line in Fig.8.

All given simulation results have been obtained by PSPICE computer simulation for parameters of one CMOS technology process [7] and supply voltages $V_{SS} =$ 0 V, $V_{dd1} = 3$V, $V_{dd2} = 6$ V, $V_{dd3} = 9$ V.

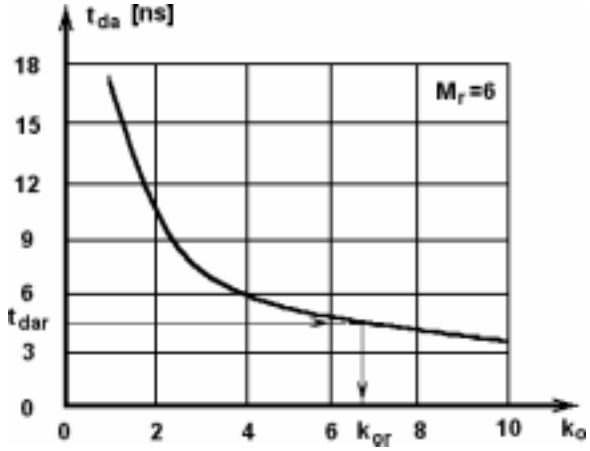


Fig. 6. Average propagation delay time as a function of ko for circuit in Fig.4.

5 Conclusions

The proposed and described designs of quaternary digital systems and circuits give the possibility for design of appropriate quaternary system and circuit depending on the need of user. There are certain possibilities that are applicable and appropriate for different needs and working conditions.

For design of quaternary logic circuits and systems practically are used similar or the same methods and procedures which are used also in the binary logic circuits and systems. One of the most important procedures in design of quaternary logic

circuits is synthesis and optimization. Here proposed and described algorithm of synthesis and optimization enables automatization of design and obtaining of logic circuits with minimal circuit area and with fulfilling needed characteristics. It is iterative and interactive process which is realized by personal computer. In principle, it can be used for all types of quaternary logic circuits. It has been practically realized and intended for synthesis and optimization of CMOS quaternary logic circuits and systems.

The proposed methods and procedures for synthesis and optimization of quaternary logic circuits and systems are very simple.

The synthesis is based on synthesis of binary logic networks since it is necessary to synthesize three CMOS binary logic networks at the input of quaternary circuit. So, same methods as for binary CMOS logic circuits synthesis are also used here. It can be easily realized CMOS quaternary circuit with any output function.

Optimization is based on optimization of input CMOS binary circuits and optimization of quaternary CMOS output stage. The procedures are very similar as in binary CMOS circuits optimization and design.

The proposed procedures are very suitable for realization using computer, as iterative and interactive procedures. Practically the procedures have been realized by personal computer. PSPICE has been used for simulation of circuits.

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