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Voltage Controlled Delay Line for Digital Signal

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Abstract: This paper describes dual delay locked loop architecture with a mixed mode phase tuning method. The circuit accomplishes low jitter, unlimited phase shift in a large operating range, and accurate phase alignment with high resolution for relatively low input clock frequency. The architecture employs two DLL loops. The first one is digital and is used for generating coarsely spaced clock pulses, while the second is analog and is intended for accurate and precise fine phase shifting. Simulations show that this circuit has 2π radians phase shift capability, and can resolve 25ps phase error at input clock frequency of 1MHz, using 1.2μm double-metal double-poly CMOS technology.

Keywords: Microelectronics, delay locked loop, delay line, clock and phase shift.

1 Introduction

The ability to handle very high-speed data with very fine timing resolution is a significant issue in high-performance synchronous digital and mixed electronics systems. Test and measurement instrumentation, telecommunication, military, medical and process control equipment are familiar application areas that require very fine timing resolution of data sampling or generation process. Normally, in all of the above-mentioned applications, the sampling rate is usually, significantly faster than the maximum data rate, so that the data timing can be controlled or measured with precision. Some classical applications, that provide clear examples of high-precision timing requirements are time set generation in the pin electronics of VLSI automated test equipment [1], and ultrasonic liquid flow-meter [2], time-of-flight particle detectors [3] and laser range finders [4]. In these systems, the edge placement

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resolution interval is often as small as (25-600) ps and is usually smaller than the minimum pulse width by an order of magnitude or more. Logic analyzers and pulse and data generators are other examples of synchronous digital system for which the clock signal is used to define a time reference for the movement of data and generation of correct timing between different signals within that system [5]. In general, clock signals are regarded as simple control signals: however, these signals have some very special characteristics and attributes. Clock signals are typically loaded with the greatest fan-out, travel over the greatest distances, and operate at the highest speeds of any signal (both control and data), within the entire system. Since all timing and data signals are provided with the temporal reference by the clock signal, the clock waveforms must be particularity clean and sharp [6]. So, the absence of any type of clock timing control can severely limit the correct operation of the entire system and create catastrophic errors.

Delay locked loops (DLLs) and phase locked loops (PLLs) are often used in the interfaces of synchronous digital and mixed electronics systems in order to hide clock distribution delays and to improve over all system timings i.e. to minimize negative effects caused by skew and jitter of clock signals. In these applications DLLs and PLLs must closely track the input clock and, as basic building blocks, provide generation and distribution of pulses that meet stringent timing design requirements. The PLL is a higher order system and is difficult to design. Its loop bandwidth, which is critical for stable operation, can change due to process, voltage and temperature variations. In the PLL, the VCO output timing uncertainty accumulates over multiple oscillation cycles and is limited by the time response of the PLL [7]. When the equipment, as for example ultrasonic liquid flow-meter, operates under increasingly more noisy conditions (electromagnetic interference due to on/off switching of motor pumps) pulse delay variations cannot be corrected instantaneously by the PLL. In applications where the frequency multiplication is not required, a DLL is a natural choice since it is free from the jitter accumulation problem of an oscillator-based design. Conventional DLL's, however, suffer from the problem of their limited delay range ($<2\pi$ radians) since DLL's adjust only the phase not the frequency [8].

In applications, like test and measurement instrumentation, where pulse generation with fine time controlled resolution (¡1ns) in the full measuring range is required, this limitation state to designers great number of problems, especially when we operate at lower frequencies (up to 10MHz, typical for ultrasonic liquid flow-meter) [2]. One innovative design solution, that is very well suited to this type of application, based on dual-loop DLL (DDLL) operation is described in this paper. DDLL is composed from two DLL

structures. The first one is digital and is used for coarse delay tuning, while the second is analog and is used for fine delay adjustment.

In the remainder of the paper, Section 2, we describe the architecture of a conventional DLL and identify three different types of delay lines structures implemented in 1.2μm CMOS process. Section 3 discusses circuits design issues that arise in the implementation of the dual-loop DLL. Section 4 discusses the simulation results, and concluding remarks follow in Section 5.

2 DLL Architecture

2.1 Conventional DLL

A simplified block diagram of a conventional DLL is outlined in Fig. 1a.

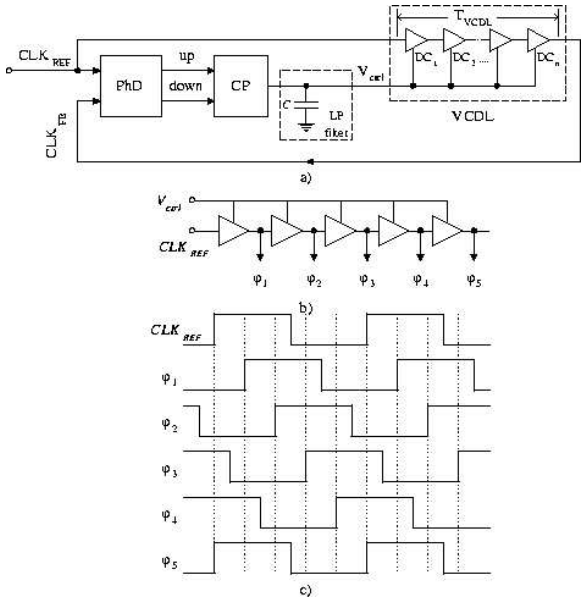

Fig. 1. a) Conventional DLL architecture, b) five-stages VCDL, c) waveform with correct lock VCDL.

This circuit contains a voltage-controlled delay line, VCDL, a phase detector, PhD, a charge pump, CP, and a first order low-pass filter. The VCDL, consisting of cascaded variable delay stages, DC_1,...,DC_n, is driven by the input reference clock, CLK_{REF}. The output of VCDL, i.e. the feedback signal, CLK_{FB}, and the CLK_{REF} rising edge are compared by PhD to determine the phase alignment error. The CP and low-pass filter integrate PhD output in order to generate a control voltage, V_{ctrl}, for the VCDL.

In normal condition, DLL forces the output clock CLK_{FB} to be aligned with the input reference clock, CLK_{REF}, through a negative feedback loop. When correctly locked, the total delay of VCDL should equal one period of the reference clock, CLK_{REF}. In Fig. 1b a five-stage VCDL is presented, while Fig. 1c shows output phases at each stage (φ_1,...,φ_5) with VCDL in correct lock.

The main problem of conventional DLL's is that they are very difficult do design to work over process, voltage, and temperature variations [9]. Since DLL's adjust only phase, not frequency, the operating frequency range is severely limited [10]. Various wide-range DLL architectures with motivation to improve their performance (i.e. operation in a wide frequency range while keeping a low jitter) have been developed [9,11-17]. Analyzing Fig. 1, one can identify that the variable delay line has a crucial role in DLL operation. Bearing this in mind, we should try, firstly, to systematize the VCDL already known from literature [9,11-17], and after that to present simulation results of several delay stage, DC_i, when they are implemented in 1.2μm CMOS technology.

2.2 Controlled delay line architectures

According to the principle of operation, i.e. a mechanism by which the delay is achieved, VCDL's can be classified into the following three categories: analog, digital and hybrid.

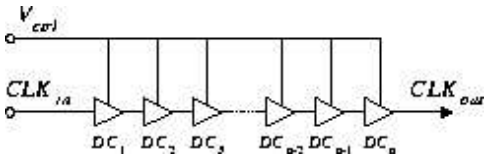

Fig. 2. Analog delay line.

2.2.1 Analog voltage-controlled delay line

The structure of analog delay line [11] is given in Fig. 2. It comprises of n cascaded variable delay buffers, DC_i, i=1,...,n.

In analog VCDL the output phase is proportional to the control voltage, V_{ctrl}, as well as the technology in which the delay buffers are implemented. Several different structures of variable delay buffers are described in [9,11-13]. Some typical realizations are diagramed in Fig. 3. The V_{ctrl+} (V_{ctrl-}) modulates the on resistance of pull-up (pull-down) transistor. These vari-

ables resistances control a current available to charge (discharge) the load capacitance. Large values of V_{ctrl} allow a large current to flow, producing a small resistance and small delay. Simulation results that correspond to

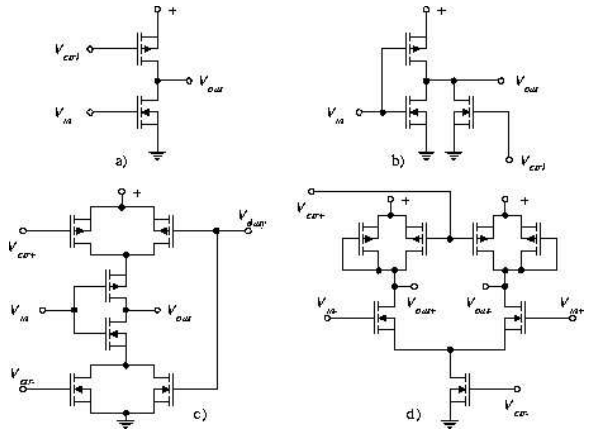

Fig. 3. Four different types of variable delay buffers.

buffer delay are presented in Fig. 4.

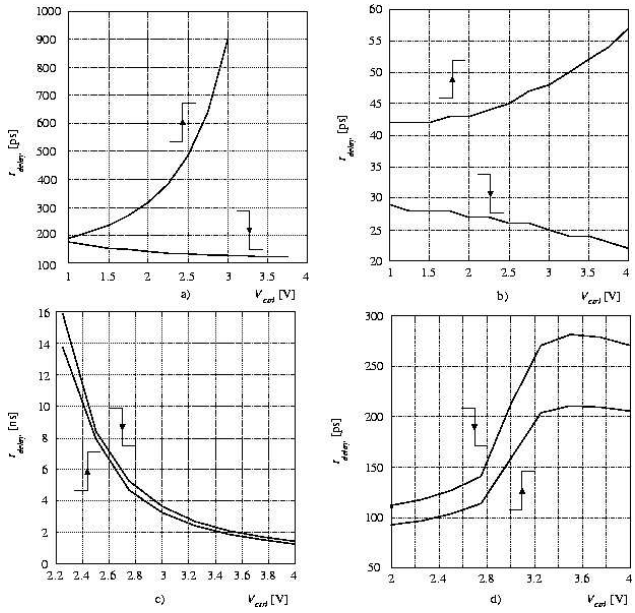

Fig. 4. Delay of analog buffer stage given in Fig. 3 in term of control voltage V_{ctrl}.

Notice: Symbols X and Y correspond to a delay of rising and falling

edges, respectively.

Conclusions concerning characteristics of variable delay buffers, given in Fig. 3, are presented in Table 1. In general, the delay buffer pictured in Fig. 3c has superior performance in respect to other realizations due to balanced delay of both rising and falling pulse edges.

Table 1. Characteristic of analog delay buffer.

properties	Circuits from the Fig. 4.			
	a	b	c	d
difference in delay between rising and falling edges of output signal	significantly unbalanced	unbalanced	relatively good balanced	balanced
duty factor corruption	yes	yes	no	yes
sensitivity to noise disturbances	large	large	relatively small	relatively small
circuit complexity	small	relatively small	complicated	the largest
delay range	small (order ps)	small (order ps)	large (order ns)	small (order ps)
operating range	small, nonlinear, (±0.2V), and asymmetrical	relatively , large (±1V), nonlinear, and asymmetrical	relatively small, linear (within a limited range), (±0.5V), symmetrical	small, strictly linear (±0.2V), symmetrical
possibility for using the circuit as delay cell or duty cycle corrector	yes (correction is related to delay)	yes (correction is related to delay)	yes (correction is independently achieved of the delay)	no

2.2.2 Digital controlled delay line

Digitally controlled delay lines are realized as multi-stage delay cells that provide fixed and quantized delay times. The switching logic selects one clock output with closest phase to the reference clock by using digital control select bits instead of using an analog control voltage. Two standard realizations of digital delay lines are known from literature [14,15]. The scheme of the first is pictured in Fig. 5. It is composed from 128 delay stages. Delay selection is performed by the MUX. Each of the delay stage involves a fixed time

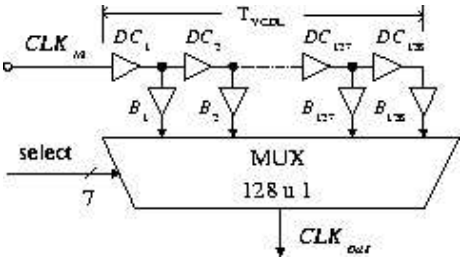

Fig. 5. Magnetic flux leakage method.

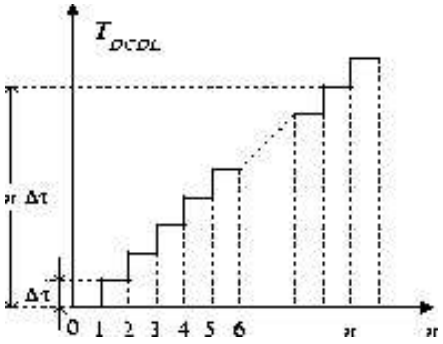

Fig. 6. The signals of inner and outer defect.

delay, $\Delta\tau$. The total time delay between CLK_{in} and CLK_{out} is adjusted to be equal to 2π radians.

The structure of the second standard solution is given in Fig. 7. The amount of the delay is determined by a content of the shift register (ShR). The delay line consists of n delay cells connected in cascade. Initially, into the ShR, information according to which the delay is determined is loaded. If the output of the flip-flop FF_i is set to logic one, while all other flip-flops, FF_j for $j \neq i$, (i, j=1..,n) are set to logic zero, the signal will propagate through the chain starting from delay stage DC_i until the stage DC_n, i.e. to the end of a delay line (this case is presented Fig. 6. with dotted lines).

In general, major drawbacks in digital delay lines are large skew, due to quantized delay time, and large jitter, due to continuous change of phase selections among quantized delay times with supply and temperature variations [9].

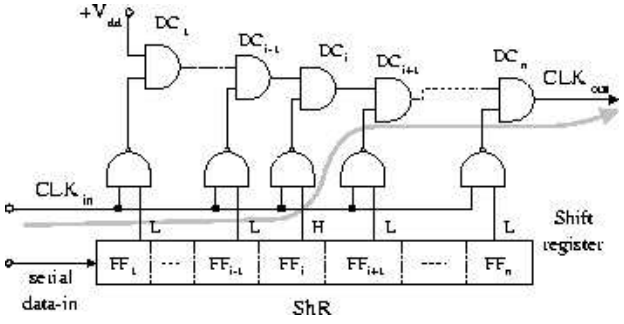

Fig. 7. Digital delay line based on shift register.

Chip area and power consumption in digital DLL's are excessive. In

addition, their jitter performance gets worse compared with analog DLL's since the number of delay stages (cells) or gates in clock propagation paths become larger.

2.2.3 Hybrid delay lines

In general, with analog delay lines, in a limited working range (0-π/16), a continual amount of high-resolution delay can be achieved. Contrary, with digital architectures discrete and coarse-grained delay, in a large operating range (0-2π radians), can be obtained. Having this in mind, most of the applications use digital delay lines for coarse, and analog for fine delay tuning. Hybrid delay lines represent a combination of analog and digital architectures. As a design choice they are good candidates for universal solutions of wide-range high-resolutions delay lines. Numerous design proposals of hybrid delay lines are described in literature [9-10,13,16-19].

Among plethora of different designs, it seems to us that the following three are of basic architecture, and more characteristics. In the first solution [16], see for example Fig. 8, a programmable coarse delay is achieved involving bypassing of delay stages. Fine delay is obtained by changing the control voltage V_{ctrl}. Each of the stage contains different numbers of delay cells, usually grouped as a power of two (i.e. 1,2,4,8,...). In a second solution [13] a two-stage combined digital-analog delay line, pictured in Fig. 9, is described. The digital delay line is used for coarse delay adjustment, while the analog one for fine-grained tuning. Delay lines pictured in Fig. 8 and 9 generate at their outputs mono-phase signals. Very often numerous applications in instrumentation and computing [17], low-power wireless communication [10,19], and others, use poly-phase clocking. In these designs [17], the delay line for coarse delay adjustment is implemented as digital, while the multiple-outputs delay lines, intended for fine-grained tuning, are realized as analog (see for example Fig. 10).

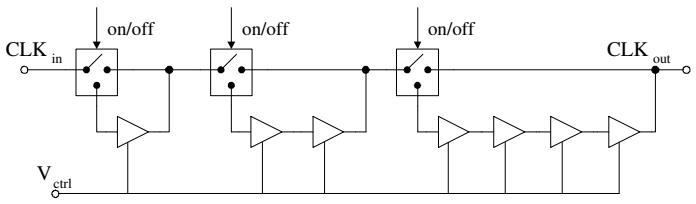

Fig. 8. Hybrid delay line.

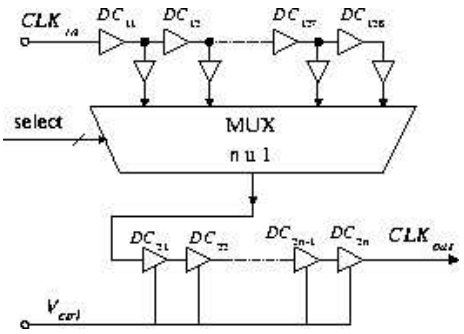

Fig. 9. Combined digital-analog delay line.

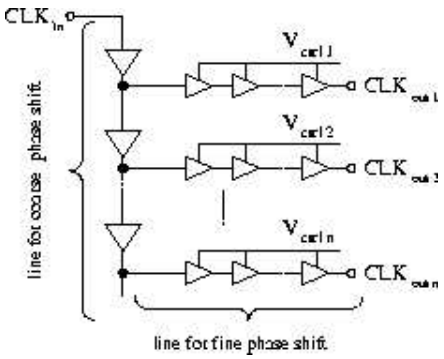

Fig. 10. Delay lines with poly-phase clock.

3 Proposed Dual-Loop DLL

Fig. 11 shows a block diagram of the proposed dual-loop DLL architecture, called DDLL. The architecture is based on two loops: a coarse-delay loop, DLL_1, and a fine delay loop, DLL_2. The phase shift between the input clock signal CLK_{in} and the output CLK_{out} can be adjusted in the range from 0 up to 2π radians. DLL_1 is a digital loop [9] and is used for coarse delay tuning in quantization steps of $(k{*}T_{CLK})/n$, where k=1,2,...,n, while DLL_2 is an analog loop, and is used for fine delay adjustment in a range from 0 up to T_{CLK}/n. Two major building blocks of the DDLL are delay lines DL_1 and DL_2. Principles of operation of DL_1, are given in [9], in more details. For our design we will adopt this proposal. Therefore, in the sequel, all our efforts will be focused to explanation of DL_2 specifics. The DL_2 in a feedback loop has similar design solution, as DL_1, but the specifics of DL_2 is that it is an analog delay line. It consists of a pair of cascaded variable delay stages with a switcher, load capacitor and comparator implemented at each delay stage. The clock signal propagates down the delay chain. The fundamental concept of the proposed delay technique is that the delay resolution is determined by the following two effects: a) a controlled charging and discharging currents of the DL_2 load capacitor; and b) alternative changes of trigger voltages at the input of the comparator during positive and negative half periods of CLK_1.

3.1 Analog delay stage - a design dilemma

Let assume that the architecture of an analog delay stage, ADS, is given in Fig. 12. As it can be seen from Fig. 12, the structure of ADS is composed from two identical current sources, I_1 i I_2, a switcher, SW, a load capacitor,

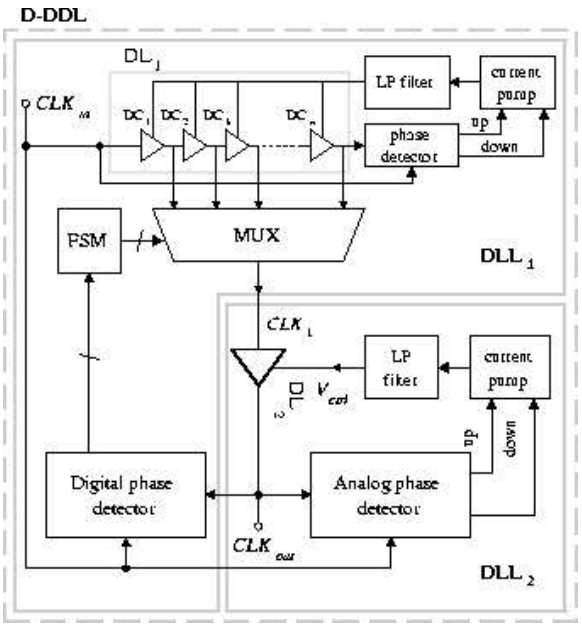

Fig. 11. D-DLL loop architecture.

C, and comparator, K. The clock signal CLK_1 controls the state of the switcher SW. When CLK_1 is high, SW switches to position 1, otherwise it is in position 2. If SW is in position 1(2) the integration capacitor C charges (discharges) with constant current I_1 (I_2).

In Fig.13, waveforms that correspond to the input signal CLK_1, a voltage across the capacitor C, and the output CLK_{out} of ADS, are sketched. In order to simplify our analysis, we will assume that the input and output signals are ideal square wave pulses, and that the duration of rising and falling pulse edges, t_{dLH} and t_{dHL}, respectively, are identical. Further we also assume, that signal propagation through the comparator K and switcher SW is fixed, and is an order of magnitude less in respect to the achieved delay. Therefore, the negative effects of these delays will be omitted.

According to Fig. 13 we see that time delays of the rising and falling pulse edges are defined by the following formulas

$$t_{dLH} = \frac{C}{I_1}(V_{H+} - V_{-}) \ , \tag{1}$$

and

$$t_{dHL} = \frac{C}{I_2}(V_{+} - V_{H-}) \ , \tag{2}$$

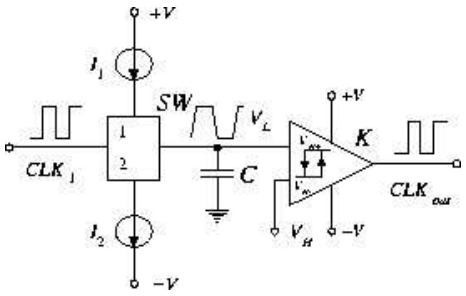

Fig. 12. Delay line architecture.

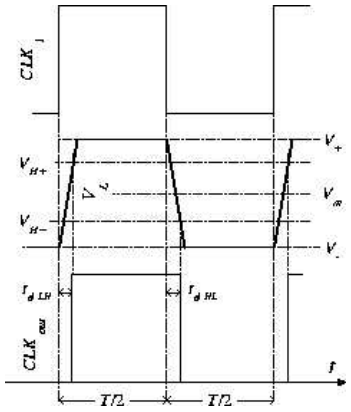

Fig. 13. Voltage waveforms in delay line.

if $t_{dLH} = t_{dHL} = \tau$ and $I_1 = I_2 = I$, we obtain

$$\tau = \frac{C}{I}\Delta V \tag{3}$$

where $\Delta V = V_{H+} - V_- = V_+ - V_{H-}$.

Concerning implementation of the ADS, our primary design goal is to achieve linear variations of the time delay but having in mind the following idea: Changes (variations) of each parameter should be individual and without visual effect to other parameters, or we can simultaneously change two or three parameters but keeping in that a satisfactory compromise. In a general case, when the output quantity is considered (in our case it is delay) it is necessary to gravitate towards the goal that variation of one parameter should be orthogonal (without influence) to changes of other parameters.

According to (3) the adjustable time delay, τ, can be achieved by controlling variations of the following three candidates, C, I and ΔV. The delay τ is proportional to the load capacitor C and voltage difference ΔV, while is inverse function in respect to the current I.

Let note that the load capacitor C can be integrated as MOS capacitor [20]. Large delay can be achieved with voltage variation V_2 (see Fig. 14.). However delay time versus control voltage is not a linear function, so this solution does not represent a good design choice.

The output voltage waveforms obtained in a case when the current I vary, in a linear fashion, are given in Figure 14. As can be seen from Fig. 14 the corresponding delay variations are not linear. Bearing in mind equitation (3) the effect of this result is real and expected. Now, again, a design decision to vary the parameter I is not a good choice.

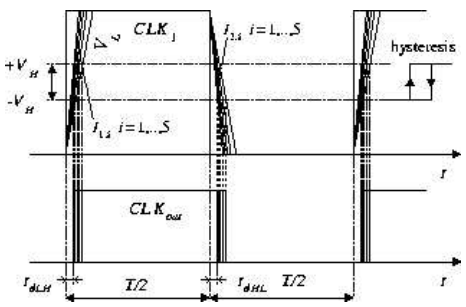

Fig. 14. Voltage waveforms in delay line with change current I.

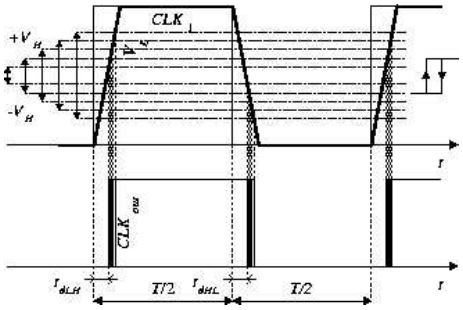

Fig. 15. Voltage waveform in delay line with voltage change ΔV.

Finally we can change the voltage difference. This can be achieved by changing a threshold of the hysteresis voltage during the positive and negative half period of a clock signal CLK_1. Fig.15 shows the effect of a signal delay versus threshold voltage variations for a circuit sketched in Fig. 12. As can be seen from Fig. 15 delay variations are linear. Having this in mind, our design choice is based on changing the voltage difference, ΔV.

3.2 Analog delay line: circuit description

At principal level Fig.16 shows a block scheme of the proposed analog delay line. The following three building blocks are constituents of the delay line: a) an integrator, IN, (its structure is identical to one depicted in Fig 12); b) a generator of threshold voltages, GH; and c) a comparator, K. At the output of the IN a trapezoidal voltage waveform, V_L, is obtained (see for example, Fig. 16). The block GH is composed from: i) switcher SW_2; and ii) two sources of voltage reference, V_{H+} and V_{H-}. During the positive (negative) half-period of the clock signal CLK_1, at the output of GH a reference voltage V_{H+} (V_{H-}) is generated. The block K compares amplitudes of signals at its inverting and non-inverting inputs. Depending on their magnitudes, square wave pulses are generated at the output of K. Time-delay variations of square wave pulses that correspond to CLK_{out} are sketched in Fig. 15. The major design problem that arises now relate to stable and accurate/precise generation of threshold voltages in a whole operating range of the proposed circuit. In a concrete case, the proposed design solutions that fulfill this condition, is pictured in Fig. 17. The circuit is composed from three transistors, M_1, M_2 and M_3. Transistors M_1 and M_3 act as dynamic resistances. A control voltage V_{ctrl} drives the input of transistor M_2. The time-delay of the output signal, CLK_{out}, is proportional to a magnitude of

V_{ctrl}. Threshold voltage V_{H+} and V_{H-} (see Fig. 17) are outputs of this circuit.

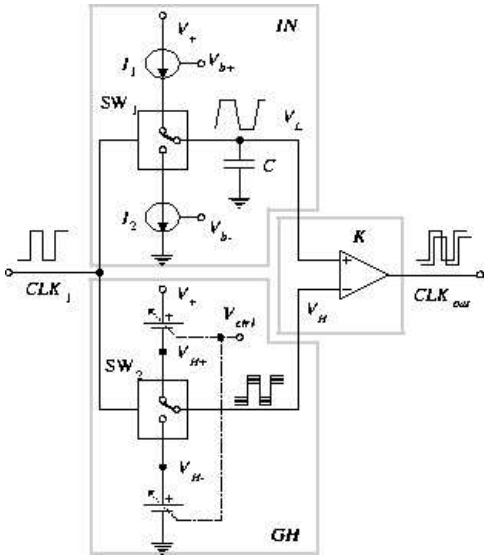

Fig. 16. Delay line principle scheme.

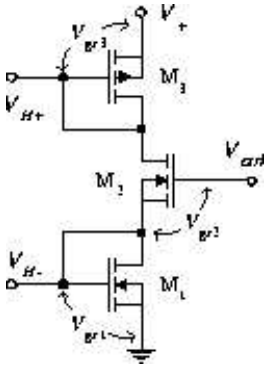

Fig. 17. The scheme for tuning of hysteresis voltages V_{H+} and V_{H-}.

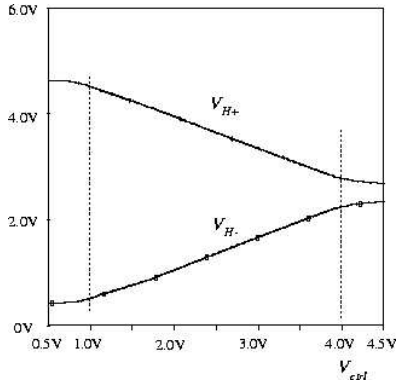

Fig. 18. Variations of VH+ and VH- in term of V_{ctrl}.

Fig. 18 shows variations of V_{H+} and V_{H-} versus control voltage V_{ctrl}. When the circuit of Fig. 17 is supplied with 5V, as can be seen from Fig. 19, if we change the control voltage Vctrl in a range from 1V up to 4V, two opposite, well balanced, voltage references V_{H+} and V_{H-} are generated.

In Fig. 19 the electrical scheme of GH is pictured. A complete scheme

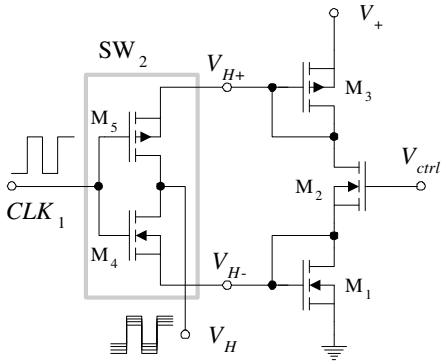

Fig. 19. Scheme of circuits for generation hysteresis voltage V_H.

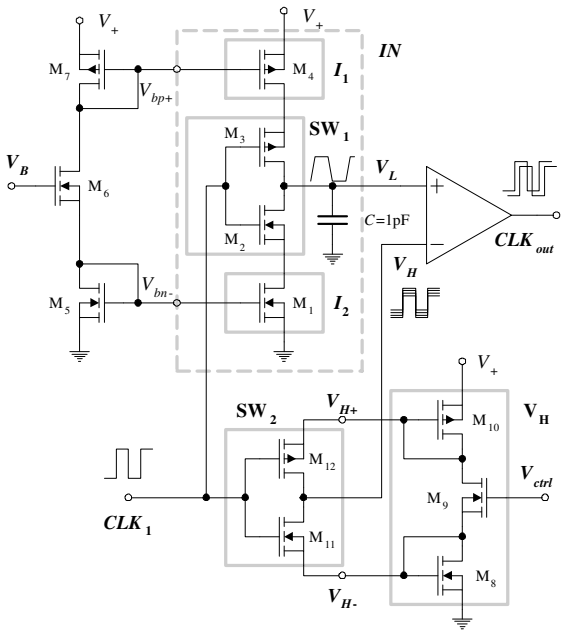

Fig. 20. Complete delay line scheme.

of the analog delay line is sketched in Fig. 20. The macro block IN pictured Fig. 20 represents a modified version of the block IN already depicted in Fig. 16. In this circuit transistors M_1, M_4, M_5, M_6 and M_7 are involved in the structure. Transistors M_1 and M_4 are used as current generators. A magnitude of the current I_1 (I_2) is determined by a bias voltage V_{bp+} (V_{bp-}).

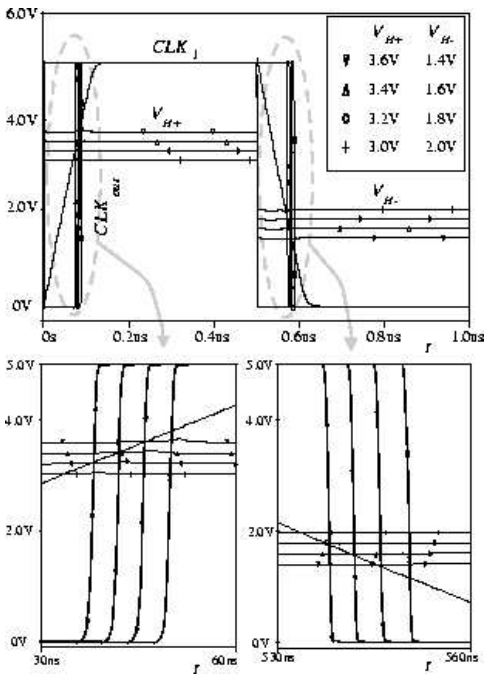

Fig. 21. Voltage waveforms in delay line get by simulation.

4 Simulation Results

Fig. 21, 22 and 23 show Spice simulation results corresponding to the voltage controlled analog delay line. The results were obtained for input clock frequency f_{CLK}=1MHz (worst case) and power-supply voltage V_{dd}=5V, as constant parameters. The simulation process was performed using circuit models in a 1.2μm double-metal double-poly CMOS technology.

Waveforms related to: a) the driving clock pulse, CLK_1; b) a trapezoidal voltage, V_L (non-inverting input of comparator K); c) hysteresis voltages V_{H+} and V_{H-}; and d) delayed output signals CLK_{out}, are diagrammed in Fig. 21. During simulation different values of the control voltage V_{ctrl} (2.8V, 3.2V, 3.6V, and 4V) were taken as variable parameters. As a consequence corresponding changes of the hysteresis voltages V_{H+} (3.6V, 3.4V, 3.2V, and 3V), and V_{H-} (1.4V, 1.6V, 1.8V, and 2V) were obtained.

Fig. 22 shows that, when the control voltage V_{ctrl} varies from 2.8V up to 4V, the delay of rising and falling edges is within the range from 39ns up to 51ns (marked with circles). A solid plotted line corresponds to an ideal case, while a doted marked line to the result obtained from simulation. As can be

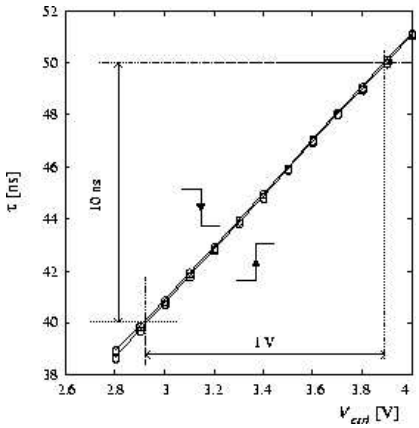

Fig. 22. Delay in function of control voltage V_{ctrl}.

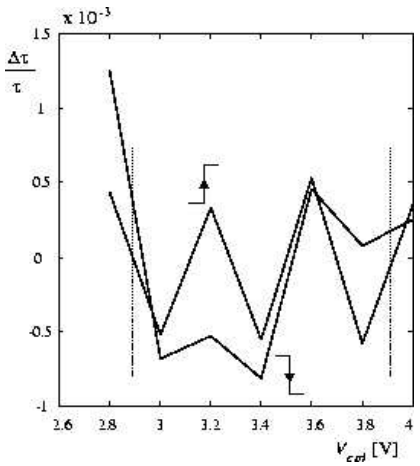

Fig. 23. Relatively variation of delay characteristic vs. linear.

seen from Fig. 21, a full range of regulation that corresponds to DL_2 is 10ns. In our case, if for input frequency of 1MHz, we want to cover a delay range from 0 to 2π radians, the digital DLL_1 as constituent of the DDLL (Fig. 11), should be composed of 128 buffer stages. Each of the stage should involve a course delay of T_{CLK}/n=1000ns/128=7.8125ns. In order to achieve good linearity and high delay resolution, the operating point should be located in the middle of the range of regulation, that corresponds to V_{ctrl}=3.4V. In this case, maximal allowed excursions of V_{ctrl} should be within a range from 2.9V up to 3.9V.

Magnitude of relative delay errors versus variations of the control voltage, for rising and falling edges of CLK_{out}, are pictured in Fig. 23. As can be seen from Fig. 23, within a regulation range of interest, the maximal relative error, $\Delta\tau/\tau$ is less than 0.05%. This result corresponds to delay resolution of 25ps.

5 Conclusion

The delay line method described in this paper requires standard digital CMOS process. This has advantages of relatively small cost, low-power dissipation, and high integration level. A high resolution is obtained by utilizing a double delay locked loop, and a voltage controlled digital and analog buffer delay stages as a time unit. At a global design level a DLL is used to stabilize the value of the buffered delay stages against process variations, temperature, and power supply changes. The described system is primarily

designed to work properly in a frequency range from 1 up to 10MHz, which corresponds from 1μs down to 100ns. Taking into account that for standard CMOS process the resolution of DLL based on a single delay line is limited to a few hundred pico seconds, in order to fulfill the design specification, our design proposal was based on usage of a double loop DLL. This approach allows us to improve the resolution. In a DDLL two DLL structures are used. The first, DLL_1, is digital and is used for coarse delay timing, while the second, DLL_2, is analog and is used for fine delay adjustment.

The simulation results show that in the worst case, at relatively low frequencies (1-10MHz), in a wide operating range (0-2π radians), a high-resolution delay (25ps) can be achieved, when the proposed solution is implemented in 1.2μm CMOS technology.

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