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# Layout Considerations for High Temperature SRAM Cells in a SOI Technology

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**Abstract:** Silicon-on-insulator technologies are well suited for high temperature circuit design, due to low leakage currents. The reduction of leakage currents is especially important in large repetitive structures such as memories. This paper describes the layout development of a high temperature SRAM cell in a SOI Technology.

First, the differences between SOI technologies and standard CMOS processes are presented. It is then discussed, how SOI specific circuit element behaviour affects the layout design of different parts of the SRAM cell. Solutions for SOI specific problems are presented and advantages and disadvantages of SOI technologies in static random access memory design are shown.

**Keywords:** Microelectronics, layout, SRAM cells, SOI technology, high temperature circuit.

## 1 Introduction

Nowadays, quite a large number of high temperature ASICs need embedded memories to store program code or to gather data from sensors. Mostly static random access memories are employed for this task, as they can be written quickly and do not need intricate refresh cycles.

The design of high temperature circuits does not only employ special circuitry, but is often based on special semiconductor processes as well. Silicon-on-Insulator technologies are especially well suited for the development of high temperature ASICs and embedded memories.

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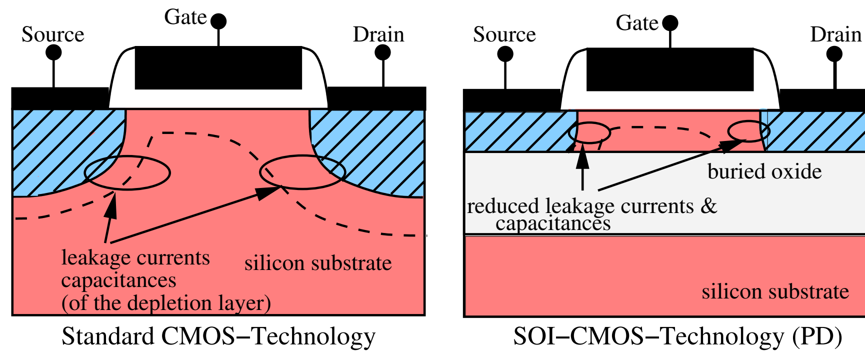


Fig. 1. MOS-Transistors in SOI and bulk-CMOS Technologies.

This article describes the differences in SRAM design between SOI and bulk CMOS technologies. An SRAM cell is being presented and SOI layout concerns for different parts of the cell are discussed. An example layout of a SRAM standard cell will be introduced and compared to cells in bulk CMOS technologies with the same scale of integration.

## 2 Silicon-on-Insulator Technologies

A SOI wafer consists of three layers. On the top a thin ($0.1 \dots 0.3\mu$m) monocrystalline silicon layer can be found above an oxide layer of $0.4 \dots 2.0\mu$m. This oxide layer is situated on a silicon handle wafer of $300 \dots 600\mu$m. The three most widely spread procedures for the production of SOI wafers are SIMOX, ELTRAN and UNIBOND. Detailed descriptions of them can be found in [1,3]. The first very thin silicon layer is used as active layer, in which the devices are being realised. The further processing of the wafers varies from bulk CMOS technologies only in one point: all devices are separated from each other by etching through the active layer down to the buried oxide. This ensures the reduction of unwanted electrical interaction between devices (cross-talk). A cross section through a SOI-MOSFET can be seen in Figure 1.

In comparison to a conventional MOSFET the vertical structure is limited by the buried oxide and the area of the pn-junctions is strongly reduced. This leads to reduced parasitic capacitances and low leakage at the pn-junctions. One of the main problems in SOI process-integration is the suppression of parasitic sidewall and backside transistors, which exist at the etching trenches and the backside of each device. Those parasitic transistors

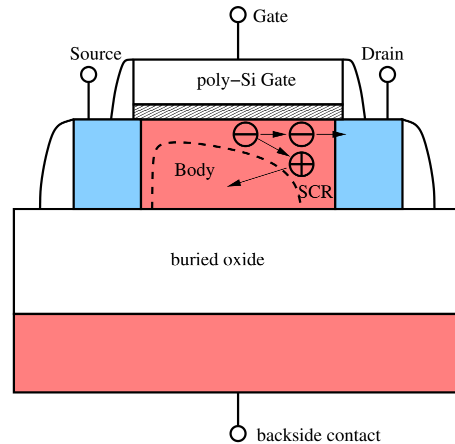


Fig. 2. The physical reason for the Floating-Body-Effect.

have a different threshold voltage than the main device and can therefore affect the ideal device behaviour. Those parasitic devices have to be suppressed technologically to minimise the negative effects.

As can be seen in Figure 2, the active area below the poly-silicon gate (body) is not necessarily contacted in SOI-devices. This leaves the possibility to either contact this area with a sidecontact or leave it floating. Having a closer look at the inner electronic processes in the transistor, it can be seen that the electrical field in the transistor during normal operation is highest at the drain side. For high drain voltages avalanche generation of electron hole pairs takes place in this area of high field strength. The charge carriers which are of the same polarity as the channel charge carriers discharge together with those through the channel to the drain. The other polarity remains in the body and charges it up. This leads to a threshold voltage shift towards lower values and increases the output current at the oxide surface (kink-effect). Therefore, the device behaviour of transistors with unconnected body depends not only on environment and technology but also on the device history, which complicates its usage.

It is in most cases desirable to suppress the kink effect by connecting the body. The kink effect can be suppressed in n-channel devices by connecting body to ground and in p-channel devices by connecting body to supply voltage. Devices with such a body contact are called "body-tied" the others are known as "floating body".

More information on the kink-effect and its causes can be found in [1,3,4].

The body tied transistors can be distinguished further, depending on the situation of the body contact:

- Body tied to source (A-Type transistor)
- Body tied to supply voltage or ground (H-Type or T-Type transistor)

A sample layout of each type of SOI transistor can be found in Figure 3.

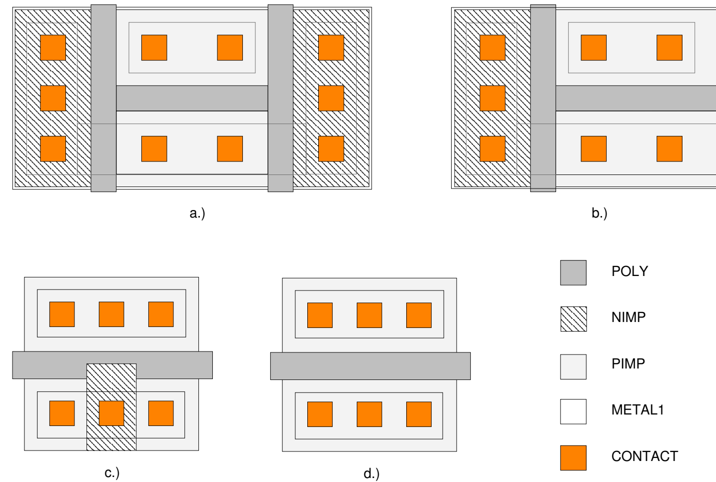


Fig. 3. a. H-Type, b. T-Type, c. A-Type, d. floating body

Both types of body ties are well suited for different kinds of applications. The body to source tied transistors are especially designed for digital applications as standard CMOS logic. Only this application ensure the proper connection of the body to either ground or supply voltage, depending on the transistor type. They are also called unidirectional transistors, because their source node can only be connected to a very limited range of values to ensure proper transistor behaviour.

H-Type transistors, with their extra body contacts at the sides of the transistor, are best used as switches or in any kind of analogue circuits. Their layout allows the body contact to be connected to ground or supply voltage independent from the source connection.

## 3 Static Random Access Memory Cells

Various types of SRAM cells can be found in literature [2, 5]. The cell best suited for use in extreme environments is a six transistor PMOS load cell.

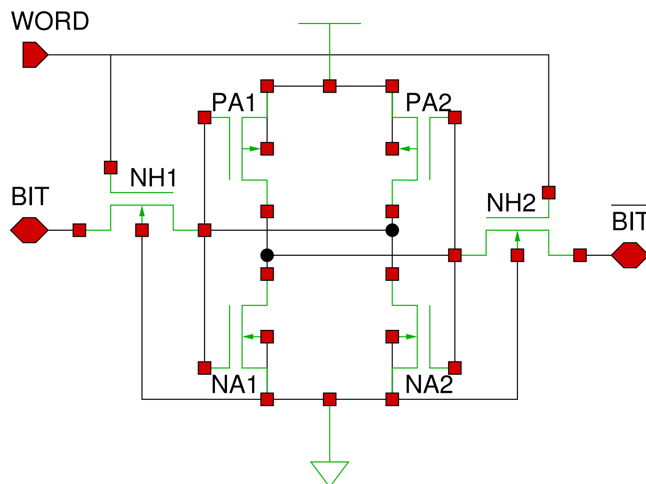


Fig. 4. Schematic of the 6-transistor SRAM cell

Each of those static random access memory cells consists of two cross coupled (latched) inverters and two access transistors. The inverters have two stable states and can therefore store one of two values. The cross coupling ensures firstly the stability of each state and secondly fast switching between states during a write cycle, as the two inverters pull each other into the next stable state. The access transistors are included in order to allow addressing of each cell in a matrix. They connect the inverter inputs to the datalines. As differential readout is more stable than single line readout [6], two access transistors are needed per cell, one for each inverter input. A schematic of the six transistor SRAM cell can be seen in Figure 4.

The access transistors are named NH1 and NH2, the cross coupled inverters are NA1, NA2, PA1 and PA2. In the transistor names, N and P refer to n-channel and p-channel devices, while the second letter H or A refers to the type of body contact used. Why these body contacts have been chosen will be explained in the next section. The function of the cell is as follows:

The **write cycle** starts with charging the bit lines to the value that shall be written and its complement. After that, the cell to be written is selected by switching the word voltage from ground to supply and thereby opening the cell. Once the access transistors have been opened, the bitline voltage is impressed on the inverter input as well. The inverters then switch in accordance to this input values and store the data in the stable state they reach then.

At the beginning of the **read cycle**, the bitlines are precharged to a specific voltage, which has to be calculated independently for each silicon process. The precharge voltage is a function of the threshold voltage, the threshold voltage drop over the expected temperature range and other process parameters [2]. Once bitline and negatived bitline are precharged, both lines are disconnected from all other circuits except the accessed memory cell. The bitline and negatived bitline are then charged or discharged in accordance to the value stored in the cell. This charging and discharging leads to a differential voltage between bitline and negatived bitline which can be amplified to a full swing logic signal by a differential sense amplifier.

The crucial points in SRAM cell design are:

- the reliability of the design which can be affected considerably by choosing the right SOI transistors
- the power consumption during quiescent state, which has to be very low, due to the large number of cells
- the size of the cell as it will be multiplied very often to form the cell matrix

With a SOI technology the quiescent state power consumption is automatically lower than in bulk CMOS designs, due to lower leakage currents. The other two points will be discussed separately for the different parts of the cell.

### 3.1 Design of the SRAM cell core

As was shown in the last paragraph, the SRAM cell core consists of two cross coupled inverters. These should be built from body tied transistors for the following reasons:

1. As the precharge voltage for read-out of the cell has been calculated for a specific threshold voltage, any body induced threshold voltage change would have negative influence on the memory behaviour.
2. The switching behaviour at a write operation may be slowed down considerably due to threshold voltage changes.

For these reasons a body contact can not be omitted, especially for high temperature applications, were all negative effects can be expected to be stronger.

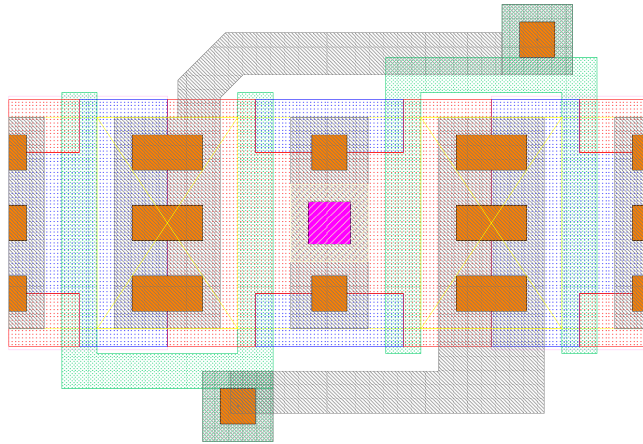

Fig. 5. Layout of an SOI SRAM Cell Core.

Now that the necessity of a body contact has been determined, a suitable method for contacting the body has to be chosen. As the source of the p-channel devices is always connected to the supply voltage and the source of the n-channel devices is always connected to ground body-to-source ties can be used. This allows to save space and simplifies the connections needed. Even more space can be saved compared to bulk CMOS designed by joining the source and drain areas that need to be connected directly instead of doing so through metal lines. This is possible in SOI because no tubs are needed. Therefore not only devices of the same type, but also the complements can be abutted to save silicon area. The layout of the complete cell core can be seen in Figure 5.

### 3.2 Cell access transistors

While body effect in the cell core mainly effects memory speed and performance, they may render the memory dysfunctional when occurring in the access transistors of the cell.

Therefore, very much care has to be taken to design the access transistors. They have to be opened reliably to pass through very different voltages. The body effect has to be suppressed completely, otherwise the resulting threshold-voltage-shift would corrupt the transistors switching behaviour. As a consequence either the desired cell can not be opened or unwanted cells may also be opened.

Apart from this problem the transistor passgate leakage could result in

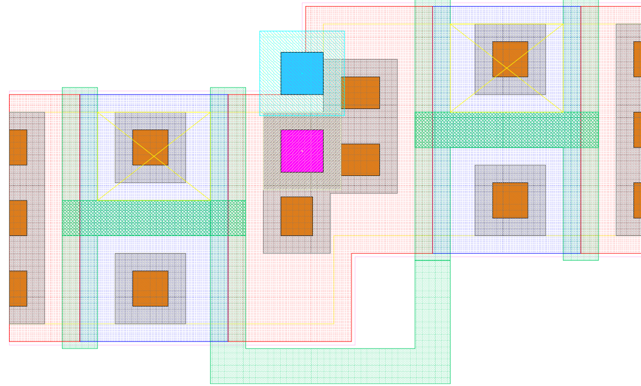

Fig. 6. Layout of SOI SRAM Access Transistors.

read or write failure. The access devices of unselected memory cells may accumulate such large parasitic bitline currents that the selected cell can not counteract them to perform the desired operation [2].

Also, area saving body-to-source ties can not be used in this case, as the source nodes can take on any voltage between ground and supply and would not provide the suitable potential to suppress the body effect. Therefore, H-type transistors have to be employed and chip area can only be saved by combining one pair of body contacts of both access transistors. The second pair sits at the upper and lower edges of the cell and will be shared with access transistors of adjacent cells of a matrix. This is possible because they both connect to the same potential.

### 3.3 Layout of the SRAM cell matrix

The previously described parts need to be put together in the most compact way possible. As has been mentioned before, a lot of space can be saved by sharing contact holes between transistors with common connections. Therefore, all source and drain areas at the edges of the memory cell will be combined with those of neighbouring cells. In Figure 7 this can be seen from the half contact holes at the cell margins. These will be completed by their cell neighbours once the matrix is put together. Special margin cells have to be created to complete the RAM cells at the edges of the matrix.

All necessary outside connections, like supply and ground voltage and data- and wordlines are realised by a grid of metal lines in three different metal layers. Hence, the supply voltage is spread evenly through the cell

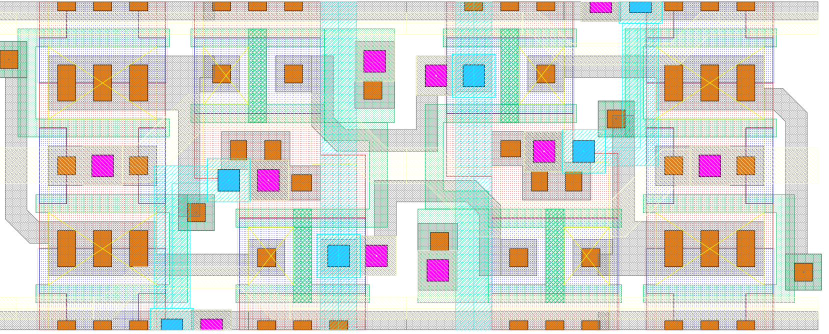

Fig. 7. Layout of SOI SRAM matrix element resembling two bits.

matrix and the signal connections for each cell can conveniently be reached from the matrix edges. No additional inter cell routing is necessary.

## 4 Conclusion

Silicon-on-Insulator technologies hold area advantages for inverter design and other logic level designs, where body-to-source ties can be used. For switches or other analogue level devices with body-to-ground ties the area consumption is considerably larger.

For SRAM cells, which include both types of devices, the area advantage of the first is consumed by the larger area of the latter. Therefore, SRAM cells produced in SOI technologies can compete with those from bulk CMOS processes in area, while at the same time providing the advantage of lower leakage currents and reduced device parasitics. The low leakage currents do especially provide advantages for designs for higher temperatures, where it keeps standby current consumption of the memory cell array down. To conclude, it can be said that SOI Technologies are ideally suited for the design of SRAMs for use at high temperatures, if the SOI specific device behaviour is kept in mind and care is taken to form a SOI compatible layout.

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