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Low-Voltage 0.35-μm CMOS Wideband Operational Transconductance Amplifier

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Abstract: A low voltage CMOS wideband operational transconductance amplifier (OTA), using regulated cascode structure with an active positive feedback, frequency-dependent current mirrors and feedforward techniques, is presented and analyzed. Such techniques stand as a powerful method of gain, bandwidth, output impedance and phase margin enhancements. In this paper, an efficient implementation of a high output impedance current mirror is used in the design of an OTA by means of the regulated cascode circuits. This amplifier operates at ± 1.25 V power supply voltage, exhibits a voltage gain of 68 dB, and provides a gain bandwidth product of 166 MHz. It drives a capacitive load of 1.6 pF and gives a power dissipation of 8.5 mW. The predicted performance is verified by simulations using HSPICE tool with 0.35 μm CMOS TSMC parameters.

Keywords: Wideband amplifiers, CMOS technology, analog Integrated Circuits, low voltage regulated circuits, gain-bandwidth product (GBW).

1 Introduction

Recently, significant efforts have been invested in reducing the power consumption of the operational amplifiers and in developing circuits that operate with extremely small voltage supplies. The trend toward implementing systems with low supply voltages has created challenging task in the design of modern analog circuits. The realization of high-speed, high gain, large gain-bandwidth product, and low power amplifiers [1, 2, 3, 4] demands innovative circuit design techniques and advances in integrated circuits process

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technology. Modern CMOS processes have carried the promise of low power and high integration levels and become attractive even for some applications that were traditionally built with bipolar transistors.

As MOS channel length decreases, the transistor cut-off frequency f_t increases and the realization of CMOS wideband amplifiers becomes more feasible [5, 6, 7]. For these, many techniques are presented to design CMOS wideband amplifiers and optimize these latter for minimum power consumption [2, 3, 8]. CMOS technology can offer a higher level of integration and has the ability of operating at relatively low supply voltages. The use of a current mirror is very advantageous for low-voltage wideband amplifier compared to a folded cascode configuration, since the latter requires an additional $V_{DS_{Sat}}$ for the common gate transistor. This $V_{DS_{Sat}}$ reduces the available output voltage, which is not negligible, especially for a low-voltage wideband amplifier.

The improvement of the high-frequency characteristics and the realization of high-output impedance are key issues in applying the current mirrors to a low-voltage wideband amplifier. However, the unity-gain frequency of the most of conventional operational amplifiers is limited to several megahertz. In order to increase the GBW of amplifiers, frequency- dependent current mirrors technique [9] has been used.

A classical approach, which increases the gain of a circuit without affecting the frequency characteristics, is the insertion of cascode stages. This technique is widespread for CMOS amplifiers, since the high output impedance of a cascode driving a MOS gate can accomplish very high voltage gains. The cascode stages reduce the output voltage swing by its drain- source voltage. This again demands a high supply voltage.

In this paper, a CMOS OTA that operates at low supply voltage, uses an active load with positive feedback [10] for both gain and bandwidth enhancements. This increase in the gain and the bandwidth is a direct result of an increase in the effective transconductance of the OTA.

The traditional cascode current output stages cannot handle a load capacitor of the order of several picofarads at low frequencies; therefore integration cannot be performed beyond this limit [11, 12]. However, choosing large C_L values of several nanofarads is not a reasonable solution, since this requires very large areas on a chip. Therefore, very high output impedance current output stages are required. The regulated cascode stage [13] was used for obtaining very high output impedance, for use in the design of high performance OTAs.

In this paper we present a low-voltage, high-gain op-amp, which can

operate with a low supply voltage. The amplifier is composed of a regulated-cascode circuits acting as composite load. The very high output resistance of these circuits allows a large dc gain for a single stage. The output biasing point of complementary regulated cascodes is stabilized in the high-impedance range, which will allow to reduce *the supply voltage* to about $2|V_T| + 2|V_{ds,sat}|$. This makes it possible to design high-gain op-amps operating at such a low supply voltage. The bias current is pulsed to improve the speed when the load has to be supplied with large amounts of charge, the limited slew rate will considerably increase the settling time if the amplitude of the input voltage step exceeds a few hundred millivolts.

2 The Proposed OTA with the Regulated Cascode Stage

Regulated cascode circuits [13, 14] contain very attractive features. In particular, extra high output resistance can be obtained, allowing the dc gain enhancement of an amplifier without needing to add additional stages [8]. A major advantage of this design approach for high-gain achievement is that Miller compensation is not needed to ensure stability, thus providing higher frequency performance [15]. Another interesting aspect of regulated cascode, which is important for low-voltage applications, is its low compliance voltage, compared with those having comparable output resistances such as triple cascode. However, to form a high resistance node (output), complementary regulated cascodes are required. Due to the enhanced output resistance, the output biasing point is unstable and highly sensitive to supply voltage variations and complementary device mismatches. It results in dc biasing deviation and unwanted ac coupling. To overcome this drawback, we employ a technique consisting of replica- regulated cascode for bias sensing and common-mode feedback for bias stabilization. A building block has been built to be used as composite load of the input stage.

The operating principle of the regulated cascode circuit shown in Fig. 1 is briefly described as follows: Transistor M_1 converts the input voltage V_{in} into a drain current I_{out} that flows through the drain-source path of M_2 to the output terminal. To obtain a high output resistance, i.e., to suppress channel-length modulation of M_1, the respective drain-source voltage must be kept stable. In the simple, that is non-regulated cascode circuit this is done by loading the drain with the low source input-resistance of the stacked transistor M_2. In the regulated cascode this is accomplished by a feedback loop consisting of an amplifier (M_3 and I_q) and M_2 as a follower. In this way

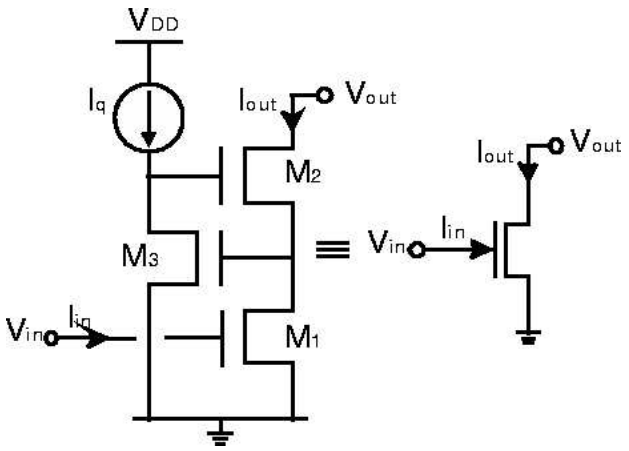

Fig. 1. The regulated cascode circuit and its equivalent transistor.

the drain-source voltage of M_1 is regulated to a fixed value. Please note that the feedback mechanism upon which the stabilization is based works even if M_2 is driven into the triode operating-region, which extends the usable range for the output signal.

In fully differential structures, better PSRR, CMRR, distortion and output swing performances are achieved.

It is possible to efficiently implement the regulated cascode stage to design an efficient operational transconductance amplifier, enabling further reduction of excess power and area consumption.

Figure 2 shows the proposed operational transconductance amplifier, which uses the regulated cascode structure as a replacement of the traditional current mirror, and this in order to improve the output impedance of the proposed OTA. In order to obtain a large GBW, transistors with large transconductance are required. Therefore, the bias currents through the input transistors have to be large. To efficiently bypass the current mirror for high frequencies, the input impedance of the current mirror should be large, while this impedance should be small for low frequencies and DC. Therefore, the frequency-dependent current mirror (FDCM) [9] is required for effective feedforward. Thus, a resistor is connected between the drain and the gate nodes of the diode- connected transistor, which forms a low pass filter with a gate-source capacitance C_{gs} of the input transistor in the FDCM. This resistor eventually delays the response but also introduces a zero, which cancels that delay. For low frequencies and DC components, the input impedance of the FDCM is low, since these components pass through the low pass filter. In

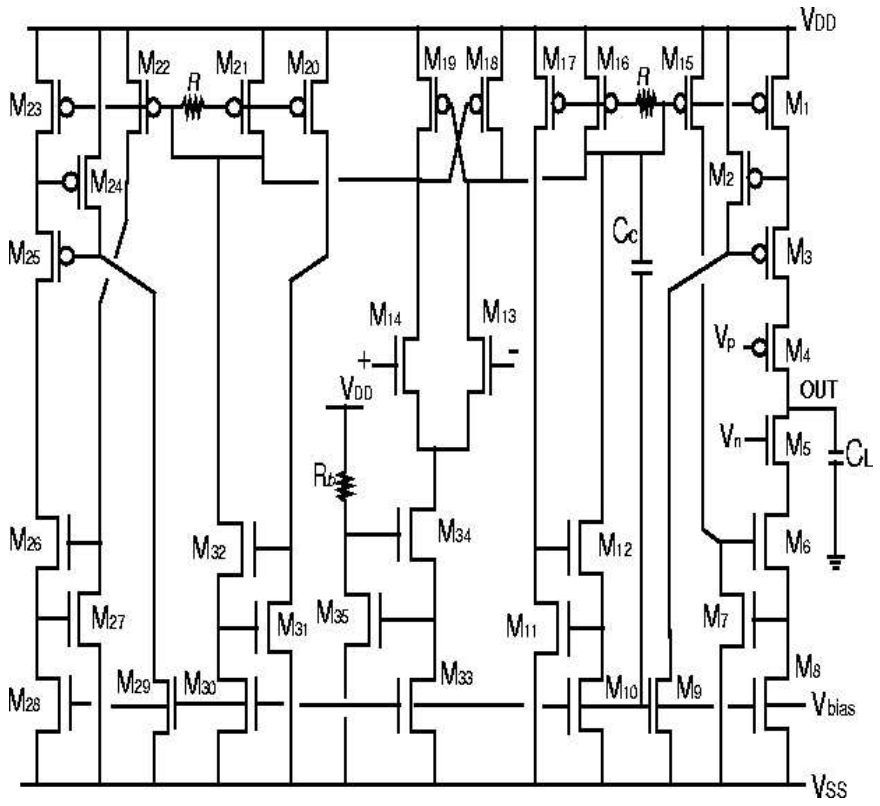

Fig. 2. The proposed low voltage operational transconductance amplifier.

this case, the FDCM operates as a conventional current mirror, where these components do not flow into the feedforward capacitor C_c, which is equivalent to an open-circuit. For frequencies higher than the cut-off frequency of the low pass filter, which is "$1/RC_{gs}$", the input impedance becomes higher since the drain-gate path is cut by the low pass filter and the transistor of the current mirror operates like a current source. In this alternate case, the feedforward capacitor behaves like a short-circuit.

The first stage of the amplifier is composed by the transistors: M_{10}-M_{14}, M_{17}, M_{20}, M_{30}-M_{32} and the diode connected transistors M_{16}, M_{21}. The second stage is formed by the transistors M_1-M_9, M_{15}, M_{22}-M_{29}. The transistors M_{18}, M_{19} form the positive feedback transistors. The transistors M_4 and M_5, which are respectively biased by the voltage sources V_n and V_p, are used for increasing the DC gain of the amplifier. The voltage gain of the

amplifier is given by

$$A_V = A_{V1}A_{V2},$$

where A_{V1} and A_{V2} are given by the following expressions

$$A_{V1} = \frac{g_{m13}}{g_{m16}} = \frac{g_{m14}}{g_{m21}}$$

$$A_{V2} = \frac{1}{2} Z_0 (g_{m_{Mpx}} + g_{m_{Mnx}})$$

$$Z_0 = \frac{rds_4 g_{m4} rds_{Mpx} rds_5 g_{m5} rds_{Mnx}}{rds_4 g_{m4} rds_{Mpx} + rds_5 g_{m5} rds_{Mnx}}$$

Mpx and Mnx are respectively the equivalent transistors of the top and bottom regulated cascode circuits composed respectively by the transistors: M_1, M_2, M_3 and M_6, M_7, M_8.

3 Simulation Results

Hspice simulations were performed for the proposed OTA. All of the simulations are based on TSMC 0.35 μm [16] twin well CMOS technology model parameters (V_{TN}=0.46 V, $V_{TP} = -0.61$ V, T_{ox}=7 nm) were used for the simulations.

Table 1. Transistors dimensions for the amplifier of Figure 2.

Transistors	W (μm)	L (μm)
M_1, M_3, M_{16}	200	0.5
M_2, M_{15}, M_{17}, M_{20}, M_{22}, M_{24}	10	0.5
M_{18}, M_{19}	100	0.5
M_4	90	0.5
M_6, M_8, M_{10}, M_{12}, M_{26}, M_{28}	84	0.5
M_{30}, M_{32}	84	0.5
M_{13}, M_{14}	1100	0.35
M_7, M_9, M_{11}, M_{27}, M_{29}, M_{31}	9	0.5
M_5	60	0.5
M_{21}, M_{23}, M_{25}	141	0.5
M_{33}, M_{34}	400	1
M_{35}	240	1

In this section, we present the HSPICE simulation results. The dimensions of the transistors are given in the Table 1. All p-channel transistors have their bulks connected to V_{DD}, and n-channel transistors have their bulks connected to V_{SS}. The Table 2 summarizes the simulated characteristics of the amplifier, which drives a capacitive load of 1.6 pF. The amplifier

operates at ±1.25 V power supply voltage with a bias current of 416 μA by means of a regulated cascode circuit, and giving a power dissipation of 8.5 mW. As illustrated in the Table 2, a gain-bandwidth product of 166 MHz and a phase margin of 62° were obtained. The gain of the designed OTA is 68 dB. The gain and phase responses of the amplifier are shown in Figure 3, and the DC transfer characteristic of the amplifier for a capacitive load of 1.6 pF is shown in Figure 4. The equivalent input and output voltages noise at 100 MHz are given in the Table 2.

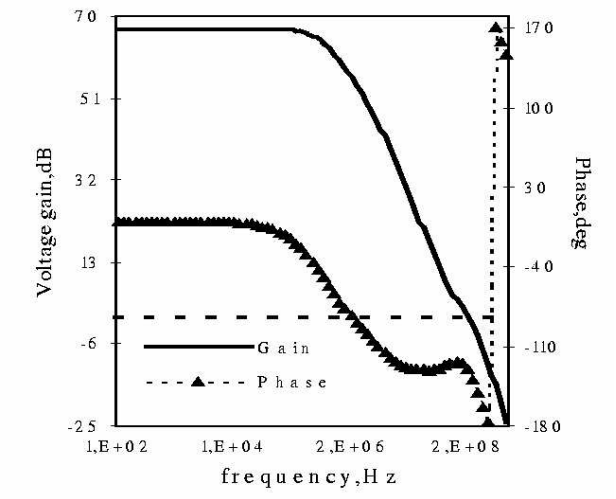

Fig. 3. Gain and Phase responses of the proposed OTA.

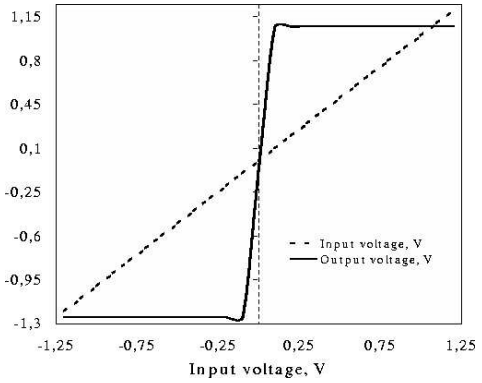

Fig. 4. DC transfer characteristic of the amplifier shown in Figure 2.

Table 2. Simulated performance characteristics of the amplifier for C_L=1.6 pF, R =780 Ω and C_c=1.8 pF.

Design parameters	Values
Power supply voltage	±1.25 V
Power consumption	8.5 mW
DC voltage gain	68 dB
Offset Voltage	5.5 mV
Unity gain frequency	166 MHz
Phase margin	62°
Slew rate	0.5 V/ns
Equivalent input voltage noise (@ 100MHz)	4.7 nV/$\sqrt{\text{Hz}}$
Equivalent output voltage noise (@100MHz)	10.9 nV/$\sqrt{\text{Hz}}$
CMRR	88 dB

4 Conclusions

In this paper, a 0.35 μm $CMOS$ low voltage wideband load compensated cascode operational transconductance amplifier, using regulated cascode structure with an active positive feedback, frequency-dependent current mirrors and feedforward techniques, has been presented and analyzed. These techniques have been applied to a ±1.25 V wideband amplifier. The essential profit and advantage of these techniques and arrangement is that the unity-gain frequency (GBW), phase margin and the gain are improved, without sacrificing the other design parameters, such as, power consumption and output voltage swing. The obtained gain is large enough for practical applications. This approach is efficient and viable to increase the gain, the bandwidth, the phase margin as well as the output impedance of low voltage CMOS OTAs.

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