

Low-Voltage, Low-Power and High Gain CMOS OTA Using Active Positive Feedback with Feedforward and FDCM Techniques

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Abstract: A low voltage, high dc gain and wideband load compensated cascode operational transconductance amplifier (OTA), using an active positive feedback with feedforward technique and frequency-dependent current mirrors (FDCM), is presented and analyzed. Such techniques stand as a powerful method of gain, bandwidth and phase margin enhancements. In this paper, a frequency-dependent current mirror, whose input impedance increases with frequency, is used to form the feedforward path at the input of the current mirror with a feedforward capacitor. By using these techniques, the gain bandwidth product of the amplifier is improved from 115 MHz to 194 MHz, the phase margin is also improved from 85° to 95° and the gain is enhanced from 11 dB to 93 dB. This amplifier operates at 2.5 V power supply voltage, drives a capacitive load of 1pF and gives a power dissipation of 7 mW. The predicted performance is verified by simulations using HSPICE tool with $0.8 \mu\text{m}$ CMOS AMS parameters.

Keywords: Wideband amplifiers, CMOS technology, analog Integrated Circuits, low power, feedforward technique, positive feedback, high dc gain, GBW.

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1 Introduction

Recently, significant efforts have been invested in reducing the power consumption of the operational amplifiers and in developing circuits that operate with extremely small voltage supplies. The trend toward implementing systems with low supply voltages has created a challenging task in the design of modern analog circuits. The realization of high-speed, high gain, large gain-bandwidth product, and low power amplifiers [1, 2] demands innovative circuit design techniques and advances in integrated circuits process technology. CMOS technology becomes attractive even for some applications that were traditionally built with bipolar transistors. As MOS channel length decreases, the transistor cut-off frequency f_t increases and the realization of CMOS wideband amplifiers becomes more feasible [3, 4, 5]. For these, many techniques are presented to design CMOS wideband amplifiers and optimize these latter for minimum power consumption [2, 4]. CMOS technology can offer a higher level of integration and has the ability of operating at relatively low supply voltages.

In the design of wideband amplifiers both in bipolar and CMOS technology, a folded cascode configuration has been widely used [3, 4, 6, 7, 8]. The reason is that the output capacitance has the same function as the compensation capacitance in this configuration. The use of a current mirror is very advantageous for low-voltage wideband amplifier compared to a folded cascode configuration, since the latter requires an additional $V_{DS_{sat}}$ for the common gate transistor. This $V_{DS_{sat}}$ reduces the available output voltage swing, which is not negligible, especially for a low-voltage wideband amplifier. The finite drain-source conductance has a large effect on the specifications of the CMOS analog integrated circuits [9]. As a result, the smaller g_0 is, the better the open loop spec is. A widely known technique to increase this g_0 is the use of the folded cascode configurations. However, the gate of cascode transistors must be correctly biased so that all transistors are always in saturation [9]. The saturation voltage $V_{DS_{sat}}$ of a MOS transistor is assumed to be $V_{DS_{sat}} = V_{GS} - V_{th}$. To avoid problems with transistor mismatches in the current mirrors, all transistors must work in strong inversion. Considering the frequency characteristic and output impedance, the current mirror produces a lower nondominant pole and a lower output impedance as compared to folded cascode configuration. Furthermore, reported improvements using feedforward techniques have been based on the folded cascode configuration [6, 10]. The improvement of the high-frequency characteristics and the realization of high-output impedance are key issues in applying the

current mirrors to a low-voltage wideband amplifier. However, the unity-gain frequency of the most of conventional operational amplifiers is limited to several megahertz. In order to increase the GBW and the phase margin of amplifiers, feedforward technique [6, 11, 12] with frequency-dependent current mirrors [13] have been used. A classical approach, which increases the gain of a circuit without affecting the frequency characteristics, is the insertion of cascode stages. This technique is widespread for CMOS amplifiers, since the high output impedance of a cascode driving a MOS gate can accomplish very high voltage gains. The cascode stages reduce the output voltage swing by its drain-source voltage. This again demands a high supply voltage.

In this paper, a CMOS OTA that operates at low supply voltage, uses an active load with positive feedback [14] for both gain and bandwidth enhancements. This increase in the gain and the bandwidth is a direct result of an increase in the effective transconductance of the OTA.

2 Low Voltage Load Compensated Cascode Operational Transconductance Amplifier

The feedforward approach on the conventional current mirror does not perform efficiently, because most of the high-frequency (HF) components of an input current flow through the diode connected input transistor, due to its low-input impedance, whereas a little amount bypasses the current mirror through a feedforward capacitor [11]. To efficiently bypass the current mirror for high frequencies, the input impedance of the current mirror should be large, while this impedance should be small for low frequencies and DC. Therefore, the frequency-dependent current mirror (FDCM) [13] is required for effective feedforward. Thus, a resistor is connected between the drain and the gate nodes of the diode-connected transistor, which forms a low pass filter with a gate-source capacitance C_{GS} of the input transistor in the FDCM. This resistor eventually delays the response but also introduces a zero, which cancels that delay. For low frequencies and DC components, the input impedance of the FDCM is low, since these components pass through the low pass filter. In this case, the FDCM operates as a conventional current mirror, where these components do not flow into the feedforward capacitor, which is equivalent to an open-circuit. For frequencies higher than the cut-off frequency of the low pass filter, which is " $1/RC_{GS}$ ", the input impedance becomes higher since the drain-gate path is cut by the low pass filter and the transistor of the current mirror operates like a current source. In this

alternate case, the feedforward capacitor behaves like a shortcircuit

Figure 1 shows a low voltage wideband load compensated cascode operational transconductance amplifier using an active Positive Feedback with feedforward and the frequency-dependent current mirrors techniques.

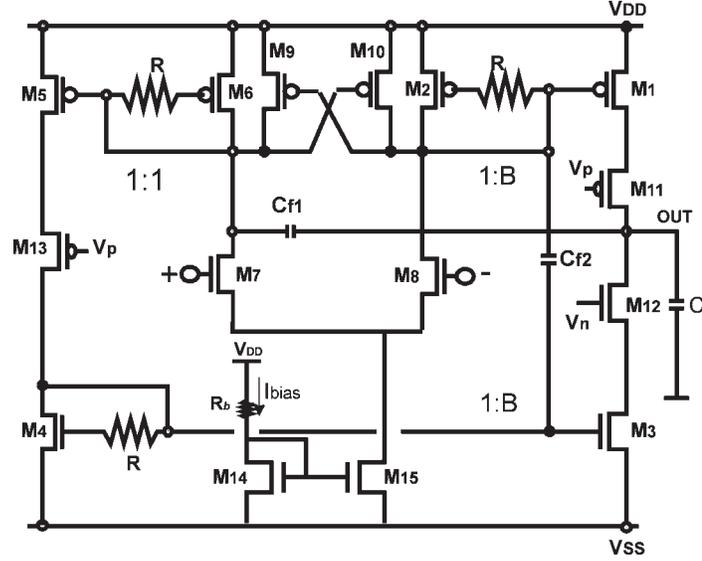


Fig. 1. Wideband Load Compensated OTA using Positive Feedback with feedforward and FDCM techniques.

The transconductance of an MOS transistor is given as follows:

- **In weak inversion**

$$g_m = \frac{I_{DS}}{nV_T} \quad (1)$$

where $V_T = kT/q$, I_{DS} is the drain-source current, V_T is the thermal voltage, k is the Boltzmann's constant, T is the absolute temperature (K), q is the electron charge and n is the weak inversion slope factor.

- **In strong inversion**

$$g_m = \sqrt{2k \frac{W}{L} I_{DS}} = \sqrt{2\mu C_{ox} \frac{W}{L} I_{DS}} \quad (2)$$

where W is the channel width, L is the channel length, k is the transconductance parameter, μ is the mobility of carriers and C_{ox} is the gate oxide capacitance.

In order to obtain a large GBW, transistors with large transconductance

are required. Therefore, the bias currents through the input transistors have to be large.

The high-frequency component of the transistor M_7 output current is fed forward to the output node directly through the feedforward capacitor C_{f1} and bypasses the two simple current mirrors which are formed by the transistors (M_5, M_6) , (M_3, M_4) , and the transistors (M_{12}, M_{13}) , which are respectively biased by the voltage sources V_n and V_p . The HF component of the transistor M_8 output current is fed forward to the input of another frequency-dependent current mirror through the feedforward capacitor C_{f2} , and is amplified. A realization with NMOS input transistors is preferable over the one with PMOS input transistors, due to the fact that PMOS input transistors requires over 30% more supply current compared to a realization with NMOS input transistors [4].

The high-frequency amplifiers require a large transconductance to drive the load capacitance up to high frequencies, and therefore consume a large amount of power. Thus, it is worthwhile to minimize this power. The transistors M_7, M_8 , which are in strong inversion, compose the first stage of the amplifier as well as the diode-connected transistors M_2, M_6 , which are maintained in weak inversion. The second stage is formed by the transistors M_3, M_4, M_{12} and M_1, M_5, M_{11}, M_{13} , which are respectively in strong and weak inversion. The transistors M_9, M_{10} form the positive feedback transistors. The voltage gain of the amplifier is given by

$$A_V = A_{V1}A_{V2} \quad (3)$$

Where A_{V1} and A_{V2} are given by the following expressions:

$$A_{V1} = \frac{g_{m8}}{g_{m2}} = \frac{g_{m7}}{g_{m6}} \quad (4)$$

$$A_{V2} = \frac{1}{2} Z_0 (g_{m1} + g_{m3}) \quad (5)$$

$$Z_0 = \frac{r_{ds11}g_{m11}r_{ds1} \cdot r_{ds12}g_{m12}r_{ds3}}{r_{ds11}g_{m11}r_{ds1} + r_{ds12}g_{m12}r_{ds3}} \quad (6)$$

3 Simulation Results

In this section, we present the HSPICE simulation results. All of the simulations are based on AMS 0.8 μ m CMOS process [15]. The dimensions of the transistors are given in the Table 1. All p -channel transistors have their bulks connected to V_{DD} , and n -channel transistors have their bulks connected to

V_{SS} . The Table 2 summarizes the simulated characteristics of the amplifier, which drives a capacitive load of 1 pF. The amplifier operates at 2.5 V power supply voltage with a bias current of 800 μ A by means of a simple current mirror, and giving a power dissipation of 7mW. As illustrated in the table 2, the unity-gain frequency is enhanced from 115 MHz to 194 MHz and the phase margin is improved from 85° to 95° . The gain of the designed OTA is enhanced from 11 dB to 93 dB.

Table 1: Transistors dimensions for the amplifier of Figure 1

Transistors	W (μ m)	L (μ m)
M ₁	282	1
M ₂ , M ₅ , M ₆	141	1
M ₃ , M ₁₂	168	1
M ₄	84	1
M ₇ , M ₈	900	0.9
M ₉ , M ₁₀	160	1
M ₁₁	382	1
M ₁₃	641	1
M ₁₄ , M ₁₅	348	1

The gain and phase response of the amplifier with and without these techniques are respectively shown in Figure 2 and Figure 3.

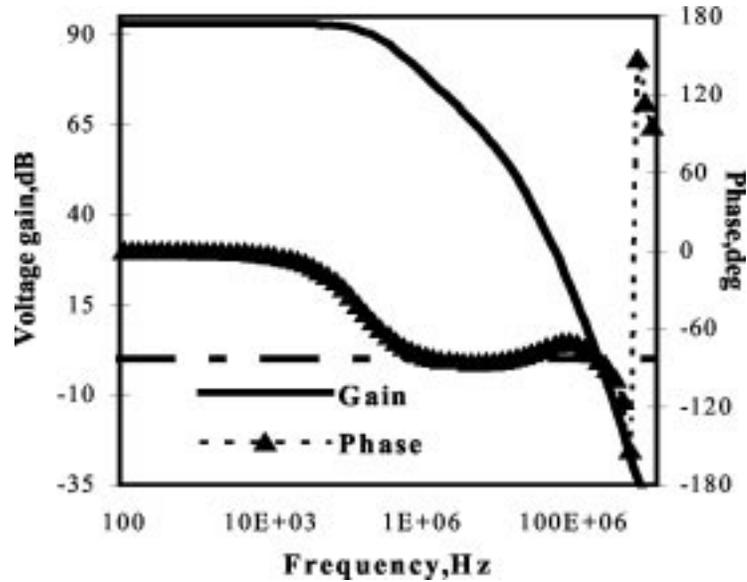


Fig. 2. Gain and Phase responses of the OTA with the techniques.

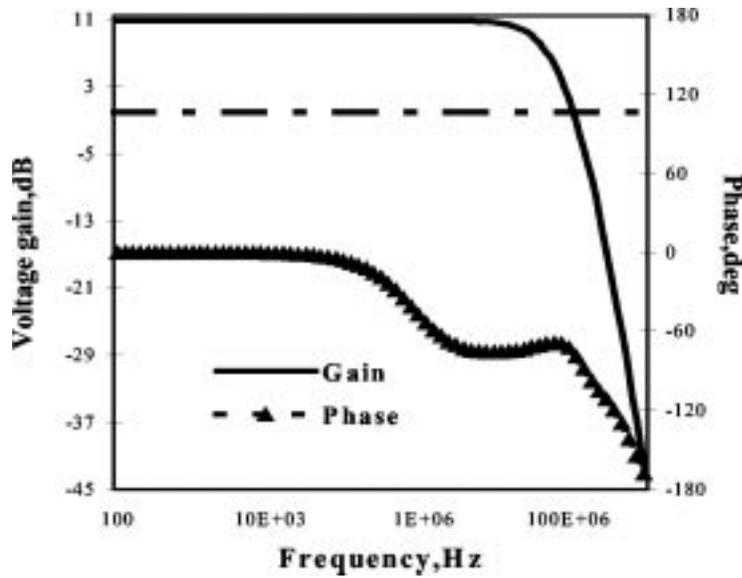


Fig. 3. Gain and Phase responses of the OTA without the techniques.

The equivalent input and output noise voltages at 100 MHz are given in the Table 2. It shows that the added resistors and capacitors cause a little deterioration of the noise performance.

Table 2: Simulated performance characteristics of the amplifier for $C_L = 1$ pF.

Design parameters	Amplifier using techniques ($R = 5$ k Ω , $C_{f1} = C_{f2} = 0.1$ pF)	Amplifier without the techniques
Power supply voltage	2.5 V	2.5 V
Power consumption	7 mW	7 mW
DC voltage gain	93 dB	11 dB
Unity gain frequency	194 MHz	115 MHz
Phase margin	95°	85°
Output Voltage swing	± 1.25 V	± 1.25 V
Offset voltage	5 mV	5 mV
Equivalent input voltage noise (@ 100 MHz)	5.03 nV/ $\sqrt{\text{Hz}}$	3.32 nV/ $\sqrt{\text{Hz}}$
Equivalent output voltage noise (@100 MHz)	28.38 nV/ $\sqrt{\text{Hz}}$	13.35 nV/ $\sqrt{\text{Hz}}$

The DC transfer characteristic of the amplifier for a capacitive load of 1 pF is shown in Figure 4.

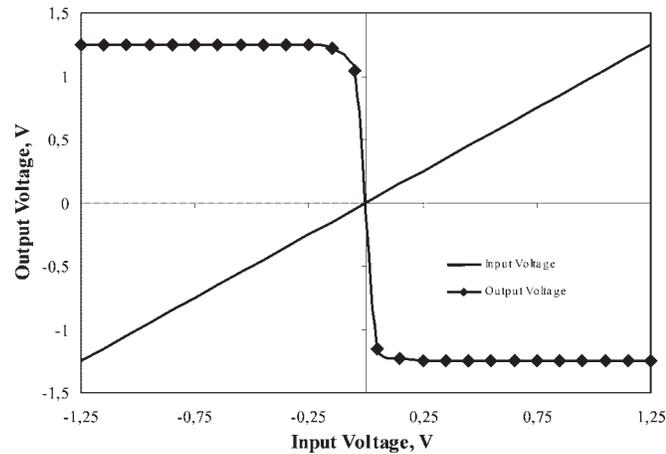


Fig. 4. DC transfer characteristic of the amplifier for a capacitive load of 1 pF.

4 Conclusion

In this paper, a 0.8m CMOS low voltage wideband load compensated cascode operational transconductance amplifier, using an active positive feedback with feedforward and frequency-dependent current mirror techniques, has been presented and analyzed. These techniques have been applied to a 2.5V wideband amplifier. The essential profit and advantage of these techniques is that the unity-gain frequency (GBW), phase margin and the gain are improved, without sacrificing the other design parameters, such as, power consumption and output voltage swing. The obtained gain is sufficient for practical applications. This approach is efficient and viable to increase the gain, the bandwidth and the phase margin of low voltage CMOS OTAs.

References

- [1] S. Sen and B. Leung: *A class-AB high-speed low-power operational Amplifier in BiCMOS technology*. IEEE J. Solid-State, vol. 31, no. 9, Sept. 1996, pp. 1325-1330.
- [2] L. Bouzerara, M. T. Belaroussi: *High gain and low-power load compensated cascode OTA using feedforward technique with frequency-dependent Current*

- Mirrors*. In: Proc. International Symposium on Signals, Circuits and Systems (SCS2001), Iasi, Romania, July 2001, pp. 93-96.
- [3] F. Op't Eynde and W. Sansen: *A CMOS wideband Amplifier with 800 MHz Gain-Bandwidth*. In: Proc. IEEE 1991 Custom Integrated Circuits Conference, June 1990, pp. 9.1.1-9.1.4
 - [4] F. Op't Eynde and W. Sansen: *Design and optimisation of CMOS wideband amplifiers*. In: Proc. IEEE 1989 Custom Integrated Circuits Conference, pp. 25.7.1-25.7.4
 - [5] P. E. Allen and D. R. Holberg: *CMOS Analog Circuit Design*, Holt, Rinehart and Winston 1987.
 - [6] W. Sansen and Z. Y. Chang: *Feedforward compensation techniques for high-frequency CMOS amplifiers*. IEEE J. Solid-State Circuits, vol.25, no. 6, pp. 1590- 1595, Dec. 1990.
 - [7] K. Nakamura and L. R. Carley: *An enhanced fully differential folded-cascode op. amp.* IEEE J. Solid-State Circuits, vol. 27, no. 4, Apr. 1992, pp. 563-568.
 - [8] L. G. A. Callewaert and W. M. C. Sansen: *Class AB CMOS amplifiers with high efficiency*. IEEE J. Solid-State Circuits, vol. 25, no. 3, June 1990, pp. 684-691.
 - [9] M. Steyaert: *An improved CMOS current mirror using a bulk-effect independent cascode biasing structure*. Circuit Theory and Design, 1989, European Conference on, pages: 656-660.
 - [10] J. H. Huijsing and F. Tol: *Monolithic amplifier design with improved HF behaviour*. IEEE J. Solid-State Circuits, vol. SC-11, no. 2, Apr. 1976, pp.323-328.
 - [11] Tetsuro Itakura and Tetsuya Iida *A Feedforward Technique with Frequency-Dependent Current Mirrors for a Low-Voltage Wideband Amplifier*. IEEE J. Solid-State Circuits, vol. 31, no. 6, pp. 847-849, June 1996.
 - [12] W. Redman-white: *A high bandwidth constant gm and slew-rate rail-to-rail CMOS amplifier circuit for embedded low-voltage applications*. In: Proc. Symposium on VLSI Circuits Digest of Technical papers, 150-151, 1996.
 - [13] T. Voo and C. Toumazou: *High-speed current mirror resistive compensation technique*. Electron. Lett., vol. 31, no .4, pp. 248-250, Feb. 1995.
 - [14] R. Wang, R. Harjani: *Parial Positive Feedback for Gain Enhancement of low-power CMOS OTAs*. Analog Integrated Circuits and Signal processing, pp. 21-34, 1995, Kluwer Academic Publishers.
 - [15] *0.8 μ m CMOS Process Parameters*. Austria Mikro Systeme International (AMS), 1997