FACTA UNIVERSITATIS (NIŠ)
Ser.: Elec. Energ. vol. 15, No. 1, April 2002, 81-92

A Novel Data Writing Method in a 1T2C-Type Ferroelectric Memory

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Abstract: A concept of a 1T2C-type ferroelectric memory, which has such excellent features as non-volatile data storage, non-destructive data read-out, and long data retention, is first introduced and it is described that in each cell of this memory two ferroelectric capacitors are connected to the gate electrode of a MOSFET. Then, the basic operation of this memory is experimentally demonstrated and a novel data writing method is proposed, which has such an advantage that the ferroelectric capacitors with the same area are well polarized, even if the gate capacitance is relatively large. A cell structure suitable for this writing method is also proposed, which has another advantage that the cell array can easily be fabricated. SPICE simulation shows that stable operation of this cell can be expected when the device parameters are optimized.

Keywords: Ferroelectric random access memory, non-destructive read-out, retention characteristics, data disturb, FET-type FeRAM

1 Introduction

FeRAM (ferroelectric random access memory) is one of the most promising memories used in portable electronic devices. So far, two types of FeRAM cells have been proposed; one is a capacitor-type or 1T1C-type cell which is composed of an FET and a ferroelectric capacitor, and the other is an FET-type or 1T-type cell which is composed of a single ferroelectric-gate

Manuscript received April 4, 2002. An earlier version of this paper was presented at the 23rd International Conference on Microelectronics, MIEL 2002, May 12-15, 2002, Niš, Serbia.

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FET. The latter cell has an advantage that stored data can be read out non-destructively. However, there is a significant problem in the 1T-type cell that the data retention time is short. In order to solve this problem, a 1T2C-type cell has been proposed, in which two ferroelectric capacitors with the same area are connected to the gate electrode of a MOSFET [1], and the basic operation of the cell has been demonstrated [2]. In this paper, a novel method to write a datum in a selected cell in the 1T2C array is discussed.

2 Cell Structure and the Basic Operation

The cell structure and the polarization directions of the ferroelectric capacitors are shown in Fig. 1. In order to write a datum in this cell, a positive or negative pulse is applied between the terminal A and B, so that the two ferroelectric films are polarized oppositely with respect to the gate electrode of MOSFET. In this case, the electric charges induced to the electrodes of both capacitors are canceled each other and no charge is induced to the gate electrode of FET, which means that no depolarization field is generated in the ferroelectric film, and the retention time as long as that of the usual 1T1C-type memory can be expected. In the cell shown in Fig. 1, the ferroelectric film thicknesses of the both capacitors are assumed to be the same. However, they are not necessary to be the same, if the polarization of the ferroelectric film is well saturated in the both capacitors.

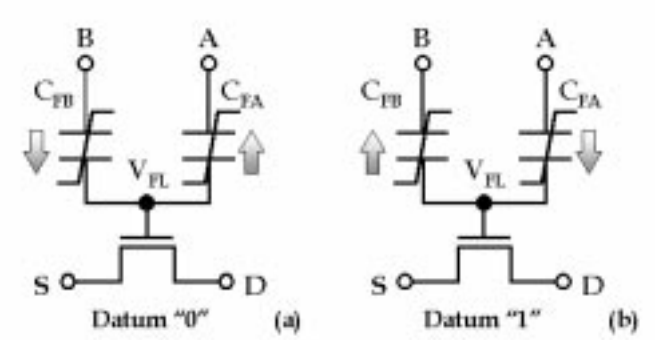

Fig. 1. 1T2C-type ferroelectric memory cell.

For the "read-out" operation, positive voltage pulses are applied to the terminal B, keeping the terminal A open. In this operation, when the stored datum is "0", no polarization reversal occurs in the ferroelectric film and a little drain current flows through the MOSFET, assuming an n-channel FET.

To the contrary, when the stored datum is "1", the polarization of C_{FB} is reversed and a large drain current flows. As discussed here, application of the readout pulses is essential to distinguished the state "0" and "1" in this cell. However, the pulse height is not necessary to be high enough to reverse the polarization of the ferroelectric film completely [2], but partial change of the polarization is preferable from viewpoints to avoid the fatigue phenomenon and to avoid the "data disturb" effect to non-selected cells.

3 Experimental Results

The 1T2C ferroelectric memory cell was designed by using a 5-μm-rule and fabricated on a silicon-on-insulator (SOI) structure [2]. $SrBi_2Ta_2O_9$ (SBT) was employed as a ferroelectric material and the memory cell was designed to be a gate-stacked structure of Pt/SBT/Pt/Ti/SiO_2/ Si (MFMOS). A 9-nm-thick gate SiO_2 layer was grown by thermal oxidation at 950°C for 15 min in dry-O_2 atmosphere. For the floating-gate electrode, Pt(60 nm)/Ti(10 nm) was deposited on the SiO_2 gate film and patterned by lift-off method. Then, a ferroelectric SBT film was deposited by the liquid source misted chemical deposition (LSMCD) method and annealed at 750°C for 30 min in O_2 atmosphere for crystallization. The thickness of the SBT film was about 150 nm. Finally, the Pt top gate electrode of 60 nm in thickness was deposited and patterned by a reactive ion etching (RIE) system using Ar gas.

"Write" and "read-out" operations of the fabricated 1T2C cell were first examined. In order to write a datum "0", V_W's (write voltages) of -4 V, 100 ms and $+4$ V, 100 ms were applied to C_{FA} and C_{FB}, respectively. To the contrary, the polarities of V_W's were inverted when a datum "1" was written. In order to read out the stored data, C_{FA} was firstly set to be open, and then the V_R (read voltage) of 2.5 V, 100 ms was applied to C_{FB}. Figure 2 shows the difference of detected drain current flowing through the MOSFET between the stored data "0" and "1". It can be seen from the figure that the on/off current ratio in the read-out operation is as high as 430 and that the current level after the read-out operation is almost the same as that before the operation. The on/off ratio of this memory cell was found to be strongly dependent on the applying conditions of V_W and V_R.

Next, the NDRO (non-destructive read-out) function was experimentally investigated. The data "0" and "1" were written by applying V_W under the same conditions as those described in Fig. 2 and then V_R of 2.5 V was repeatedly applied to C_{FB}. Figure 3 shows the variation of drain current for

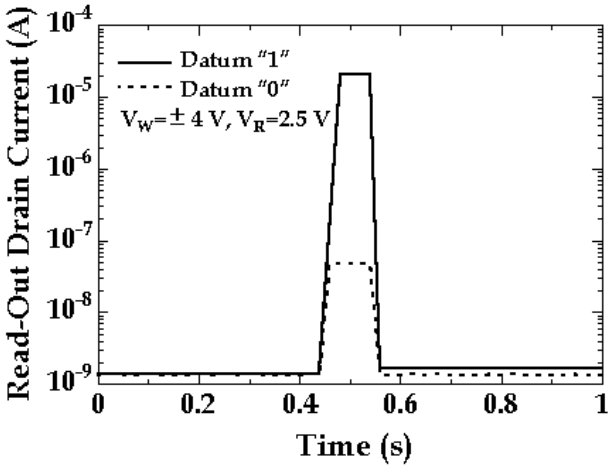

Fig. 2. Read-out operation of the fabricated 1T2C ferroelectric memory cell, when V_W was ± 4 V and V_R was 2.5 V, in which the obtained memory on/off ratio was 430.

the datum "0" (Fig. 3(a)) and the datum "1" (Fig. 3(b)) state, in which the read-out drain current of each memory state did not show a drastic change at least by 10^3 pulses. It was also found that the drain current for both data of "0" and "1" hardly changed even after 10^4 read-out pulses were applied under the same conditions. This result suggests that the polarization loss of C_{FB} for the datum "1" can be negligible for small V_R. It is inferred from these results that NDRO can be practically realized in the proposed memory cell.

Finally, the data retention characteristics of the fabricated memory cell were examined by measuring the variation of drain current with time for various polarization states. Comparison of the retention characteristic for each polarization state, which is illustrated in Fig. 4, clarifies the difference between the conventional MFMOS-FET and the 1T2C ferroelectric memory cell. The states (A) and (B) correspond to the datum "1" and "0" for 1T2C memory cell, respectively. On the other hand, the state (C) corresponds to datum "1" of the conventional MFMOS-FET, since the polarization directions of both capacitors are downward. Similarly, the state (D) corresponds to datum "0" of the conventional MFMOS-FET, since the polarization directions of both capacitors are upward. In the state (E), an adequate V_G of 0.5 V was applied to both capacitors during measurement, so that the retention characteristics were improved. The state (F) was chosen to monitor the initial state of 1T2C memory cell with time.

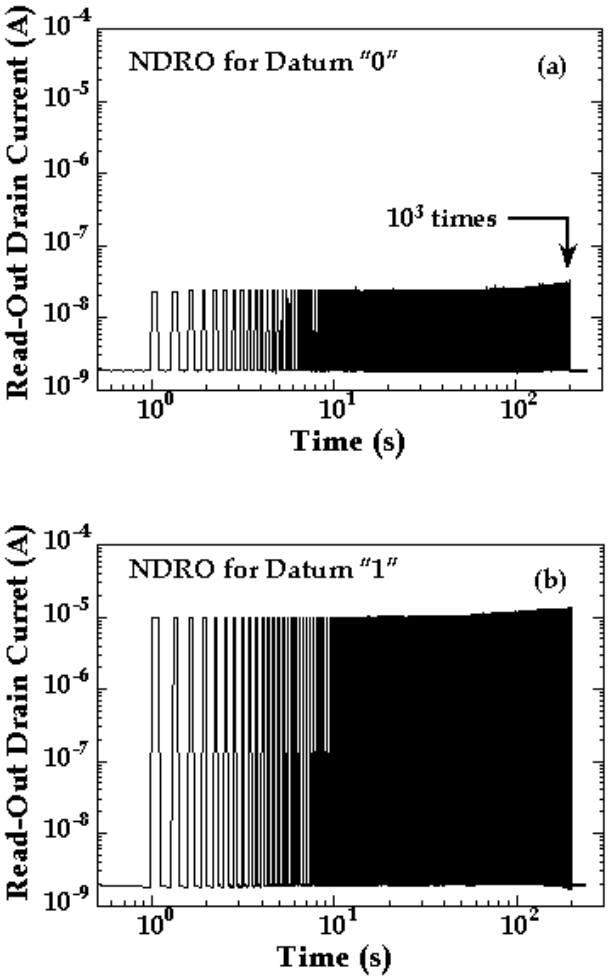

Fig. 3. Nondestructive read-out operation for (a) the stored datum "0" and (b) the stored datum "1" in which 10^3 read-out pulses were employed.

When the polarization directions of both capacitors are parallel [states (C), (D), and (E)], the binary data of "1" and "0" can be distinguished without any read-out signals, but the drain current of the datum "1" drastically decrease within 10^4 s due to the depolarization field. On the other hand, when the polarization directions of both capacitors are opposite [states (A) and (B)], the binary data can be distinguished only when the read-out pulses are applied, and the response current to the read-out pulses do not degrade at least up to 10^5 s, as shown in Fig. 4. It is concluded from these measure-

ments that the effective suppression of the depolarization field is the origin of the excellent data retention characteristics of the 1T2C memory cell.

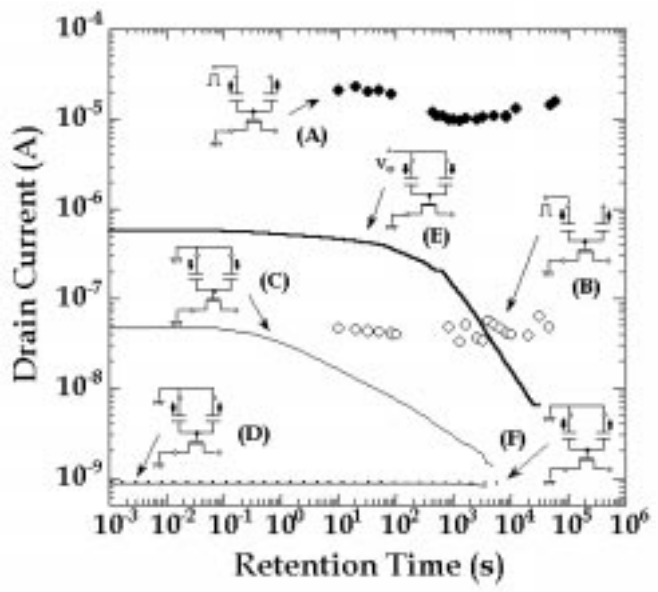

Fig. 4. Data retention characteristics of the fabricated 1T2C memory cell at various polarization states of ferroelectric capasitors. The polarization directions of capacitors and measurement conditions are as follows: (A) C_{FA}: down, C_{FB}: up [Fig. 1(b)]. (B) C_{FA}: up, C_{FB}: down [Fig. 1(a)]. (C) C_{FA}: down, C_{FB}: down, $V_A = V_B = 0\,V$. (D) C_{FA}: up, C_{FB}: up, $V_A = V_B = 0\,V$. (E) C_{FA}: down, C_{FB}: down, $V_A = V_B = 0.5\,V$. (F) Dashed line, C_{FA}: up, C_{FB}: down, $V_A = V_B = 0\,V$.

4 Integration of 1T2C Cells

In order to integrate these cells, an array structure shown in Fig. 5 is proposed [1]. In this structure, each Si stripe, which has npn region in it and is formed on an insulating film, corresponds to parallel connection of MOSFETs, and it is covered with SiO_2 and the floating gate electrodes. The capacitors C_{FA} and C_{FB} are formed between the second metal electrode and the floating gate electrode and between the first metal electrode and the floating gate electrode, respectively. As can be seen from the figure, the film thickness is different between C_{FA} and C_{FB}, but the area is geometrically adjusted to be the same. This structure has such an advantage that precise mask alignment is unnecessary. A similar structure can be fabricated

in a bulk Si crystal, if p-well or n-well stripes are formed in the crystal. In this case, however, negative voltage pulses are necessary either in "write" or "read-out" operation.

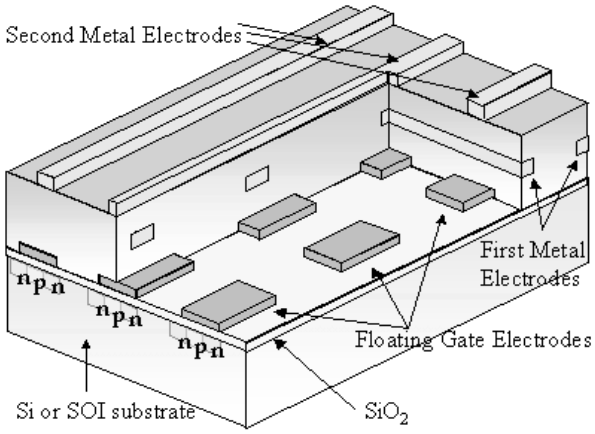

Fig. 5. Structure of 1T2C-type ferroelectric memory array with high density integration.

In order to write a datum in this array, it is necessary to apply a voltage between the first and second metal electrodes which are placed perpendicularly each other. That is, no cell selection FET is used in this array. An effective writing method in such an array is the V/3 rule, in which the applied voltage ratio between the selected and non-selected cells is 3 to 1. It is also known that the compensation operation, in which voltage pulses with the same amplitude but the opposite polarity are applied to most non-selected cells [3], is effective to minimize "data disturb" effect. Voltage pulses applied to the periphery circuit in "write" and compensation operations are shown in Fig. 6(a) and (b), respectively.

5 Proposal of a Novel Writing Method

In the data writing method shown in Fig. 6, the MOS gate capacitance C_{OX} of 1T2C cell is assumed to be negligibly small. However, in the actual structure shown in Fig. 5, the gate capacitance is not very small and the floating gate potential is kept close to the ground potential independent of the potentials of the terminals of A and B. Thus, the appropriate voltages are not applied to the both capacitors. In the worst case, for example, the polarization of the ferroelectric capacitor is reversed by application of a voltage

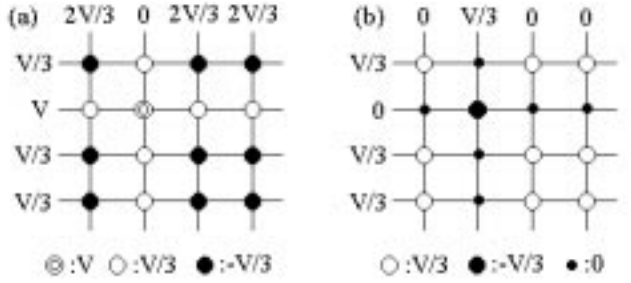

Fig. 6. "Write" operation to a cell (a) and the compensation operation to minimize the "disturb" effect (b).

pulse of 2V/3 in Fig. 6(a). Thus, in this paper, we propose and simulate the data writing method in the case where the MOS gate capacitance is not negligible. For this purpose, a novel array structure shown in Fig. 7 is proposed, in which arrangement of the Si stripes and the floating gate electrodes are the same as those in Fig. 5. Then a ferroelectric film is deposited on the floating gate electrodes and two metal electrodes are placed on the ferroelectric film in parallel. In this structure, C_{FA} and C_{FB} are formed between the two metal electrodes and the floating gate, and they have the same film thickness. This condition is advantageous from a viewpoint of fabrication process, because it is not necessary to deposit ferroelectric films twice, which was necessary in the case of Fig. 5.

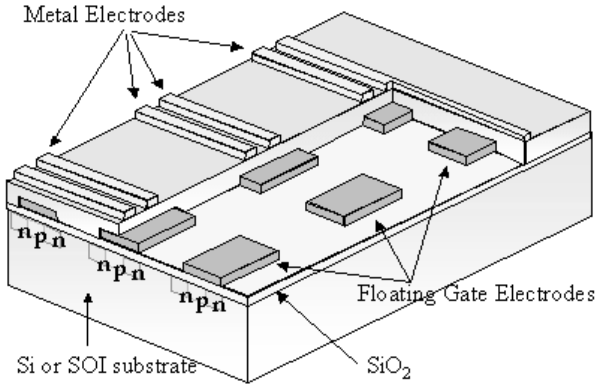

Fig. 7. A novel 1T2C-type ferroelectric memory array.

In order to write a datum "1" in a selected cell in the array, a positive voltage pulse is applied to the selected metal electrode forming C_{FA}, keeping

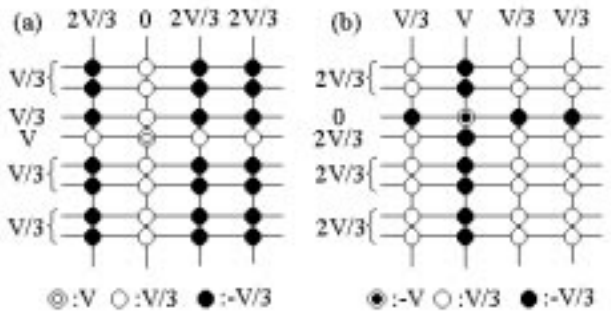

Fig. 8. "Write" operation for a proposed novel array structure. To complete the operation, the first (a) and second (b) pulses are applied successively. Vertical and horizontal lines represent Si stripes and top electrodes of ferroelectric capacitor, respectively.

the selected Si stripe grounded, and in the next timing, a negative pulse is applied to the selected metal electrode forming C_{FB}, keeping the same Si stripe grounded. At the same time, voltage pulses satisfying the V/3 rule are applied to other metal electrodes and Si stripes, in order to minimize the "data disturb" effect. This data writing method is summarized in Fig. 8, in which the above mentioned method has been realized using only positive voltage pulses. As can be seen from the figure, the compensation effect is automatically realized in almost all cells, except for non-selected cells located along the selected metal electrodes. Therefore, a particular compensation operation is unnecessary in this cell array and the same writing speed as the case of Fig. 6 can be expected. The "read-out" operation is exactly the same as that in Fig. 5. As shown in the above explanation, it is a necessary condition to use ferroelectric capacitors with the same film thickness.

6 Simulation of the Operation

In order to clarify effectiveness of the proposed writing method, we simulated the "write" and "read-out" operations for a selected cell by HSPICE model. A standard 0.6μm-gate length technology was assumed for simulating the operation of FETs. Both gate-length L and gate-width W were assumed to be 1.8 μm. In calculation of ferroelectric components, the simulation model developed by T. Tamura et al. was used [4, 5]. Remnant polarization of 6 μC/cm^2, coercive voltage of 0.7 V, and area of 0.12 μm^2 were assumed as simulation parameters of ferroelectric capacitors. Terminal voltages of the selected cell used in this simulation are summarized in Fig. 9. In this cell

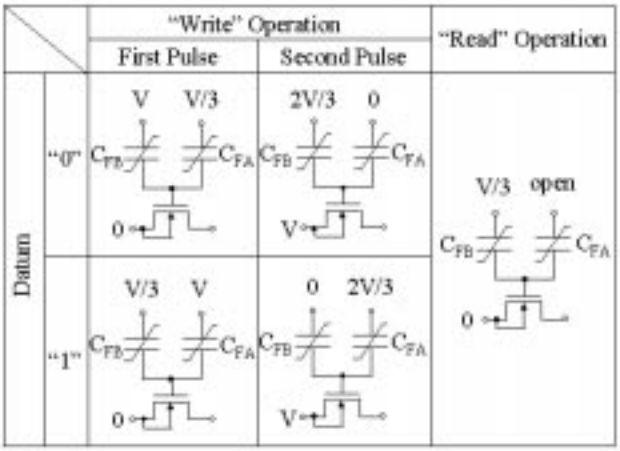

Fig. 9. Summary of the simulated terminal voltages during the "Write" and "Read-out" operations for a selected cell. For the present simulation, V=5(V).

array, since the thickness of the ferroelectric film is the same between C_{FA} and C_{FB}, there is a possibility that the "data disturb" effect in the "readout" operation is significant. Thus, in this simulation a "readout" pulse voltage as low as V/3 was assumed. The actual V value was 5 V and the drain voltage of 0.1 V was assumed during the "read-out" operation.

A simulation result is plotted in Fig. 10, in which data "0" and "1" were alternately written and they were read out 10 times repeatedly after each "write" operation. When the "write" operation is completed, polarization charges Q_{ferro} of ferroelectric capacitors A and B have almost the same absolute values, which are enough to memorize the information "0" or "1" safely, and the polarized directions are opposite each other. Consequently, the floating gate voltage V_{fg} becomes almost zero and no depolarization field is expected to generate in the ferroelectric capacitor. However, small increase of V_{fg} is still observed after being written data "1", which is probably because a part of charge remains at the floating gate of the MOSFET, based on the capacitance ratio among C_{FA}, C_{FB} and C_{OX}. Concerning the "read-out" operation, the figure shows that non-destructive read-out can be carried out. Furthermore, as we can see that the readout current ratio I_{ds}(datum"1")/I_{ds}(datum"0") over 3 orders of magnitude is successfully obtained, as indicated in the figure.

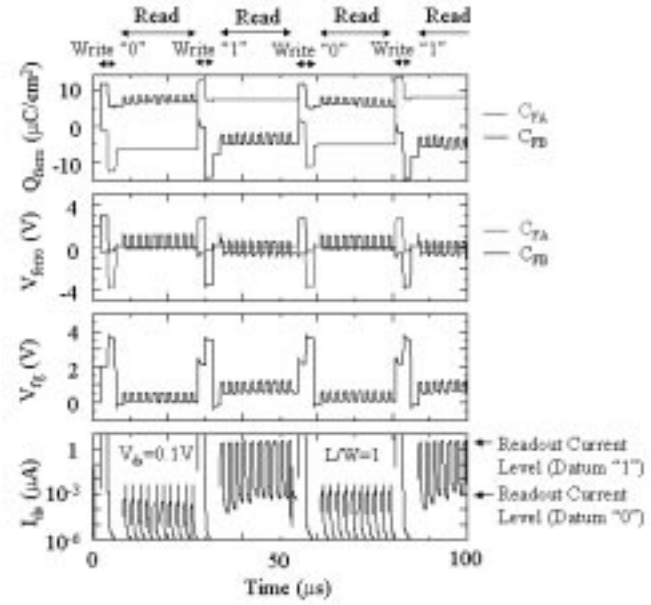

Fig. 10. Simulated waveforms of a 1T2C-type memory cell. Q_{ferro}, V_{ferro}, V_{fg}, and I_{ds} represent the charge induced to a ferroelectric capacitor, the voltage across a ferroelectric capacitor, the floating gate voltage, and the drain current of a MOSFET, respectively.

7 Conclusion

We proposed and simulated a novel data writing method of 1T2C-type ferroelectric memory. It was shown from the simulation results that the ferroelectric films were well polarized in this method, even if the gate capacitance was relatively large. It was also shown that the written data could be read-out non-destructively with the current on/off ratio over 3 orders of magnitude.

Acknowledgement

This work was performed under the auspices of R & D Projects in Cooperation with Academic Institutions (Next-Generation Ferroelectric Memories), supported by NEDO (New Energy and Industrial Technology Development Organization in Japan) and managed by FED (R & D Association for Future Electron Devices).

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