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# TECHNOLOGY, PERFORMANCE AND DEGRADATION CHARACTERISTICS OF SLS ELA THIN FILM TRANSISTORS

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**Abstract**. *Low temperature polycrystalline silicon thin film transistors (LTPS poly-Si TFTs) are essential for large area electronics and high performance flat panel displays. In recent years, LTPS TFT performance has substantially increased due to the important breakthroughs in the field of polycrystalline silicon crystallization and also due to the optimization of the process steps that differ from those of typical MOSFETs, mainly because of the requirement for low temperature procedures. In this review we present the electrical characteristics of polycrystalline silicon TFTs, crystallized with different variations of the advanced SLS ELA technique, and the determination of process technological parameters that affect the device performance, in order to further optimize the production of such high performance transistors, in terms of poly-Si microstructure, channel dimensions and topology. Also, the effect of these fabrication parameters on device degradation characteristics is studied, with an attempt to model and predict degradation characteristics*.

**Keywords**: *TFT, SLS ELA, poly-Si, LTPS, crystallization, degradation*

## 1. INTRODUCTION

Polycrystalline silicon thin film transistor (TFT) technology is critically important for large area electronics, particularly for flat panel active matrix liquid crystal display applications (AMLCDs), and for high density static random access memory (SRAM) circuits [1]. In particular, low temperature polysilicon (LTPS) TFTs have been intensively investigated because they can be used for integrating driving circuits and pixel elements on a common substrate in flat panel displays for realizing systems on panel (SOP). This is the case because LTPS TFTs have much higher electron mobility and drive current com-

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pared with amorphous-Si TFTs (a-Si) [2-4]. However, these advantages could not be fully realized in the early days of LTPS TFT technology, when solid phase crystallization (SPC) was the means of acquiring the polysilicon films; due to low-temperature processes that have to be used for glass substrates, numerous defects in poly-Si grains and at grain boundaries exist and degrade device characteristics. In recent years, these issues have been mainly overcome by using a variety of advanced crystallization processes that have been developed, such as sequential lateral solidification excimer laser annealing (SLS ELA) [2-4]. Utilizing such techniques, it is now possible to fabricate polysilicon TFTs of very high active layer quality, suitable for system on panel applications.

In this paper, we present results on the performance and reliability characteristics of LTPS TFTs obtained through various innovative SLS ELA techniques. We first briefly discuss the development of laser annealing techniques, which have yielded breakthroughs in polysilicon film quality, and then we particularly describe the SLS ELA method. Subsequently, in the experimental section we describe the particular SLS ELA techniques used, the TFT fabrication process and the electrical measurements for extraction of device parameters and characteristics for performance and reliability investigation. The SLS ELA methods we have utilized yield polycrystalline silicon grains with engineered shapes, which can be and very elongated, thus resulting in TFTs exhibiting very high performance. Moreover, they also allow the fabrication of TFTs with channels oriented in parallel or vertically to the grain boundaries, thus affording more control on TFT characteristics. In addition, the TFT structure and geometry has significant effects on device performance and reliability, which are investigated. Advanced device structures such as double gates offer additional flexibility for tailoring TFT electrical characteristics to achieve enhanced performance.

## 2. POLYSILICON CRYSTALLIZATION

### 2.1. Basic features of laser annealing techniques

Laser anneal crystallization techniques constitute a radical departure from earlier, thermal furnace based, SPC methods; they allowed TFT fabrication to overcome thermal budget constraints posed by the glass substrates and achieve drastically improved active layer film quality. A particular type of laser called excimer is mostly used for the crystallization of amorphous silicon (a-Si) films, in a process called Excimer Laser Crystallization (ELC) or Excimer Laser Anneal (ELA). These lasers use stimulated radiation from excimer molecules (each consisting of a noble gas and a halogen gas atom) in the ultraviolet range, which is very strongly absorbed by amorphous silicon; for silicon crystallization ArF, KrF, XeCl and XeF are used, emitting laser light of wavelength 193 nm, 248 nm, 308 nm and 351 nm, respectively. The incident laser energy is mostly absorbed within the first atomic layers (6-10 nm thick) of the silicon film, thus causing rapid heating and melting of the film. XeCl, emitting at 308 nm, is the excimer laser most commonly used, because at this wavelength a-Si absorbs radiation very strongly, while the cost and lifetime of relevant optics are suitable for mass production. Typical XeCl laser pulses have frequency of around 300 Hz and duration of 10 to 50 ns.

ELC of a-Si films can be classified in different crystallization regimes depending on the incident laser energy [5], a low energy (A), a high energy (C) and an intermediate energy one (B) (Fig. 1). In the first case, the laser energy is sufficient to only partially

melt the silicon film, while in the second one the energy is high enough for full melting. Within a narrow process window in between lies the intermediate regime, which corresponds to the situation of superlateral growth (SLG). This is a mechanism of great technological importance, as the polysilicon film formed has grains significantly larger than the film thickness. In this case, we have near-complete melting in which there are discrete islands of still solid material under the molten silicon, separated by fully melted material. These solid islands constitute crystallization seeds, from which lateral crystal growth within the surrounding molten silicon commences. Conventional ELC aims at near-complete melting for SLG and, via repeated irradiations, increase of size and uniformity of the grains. Multiple irradiations may use some overlap, between shots, in the exposed area; the number of shots and the overlap width are determined by film quality and throughput considerations.

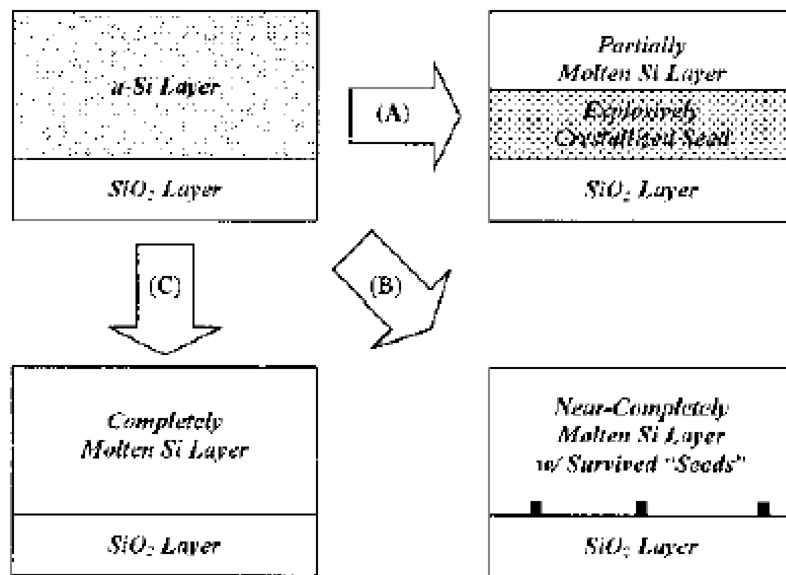


**Fig. 1** The three crystallization mechanisms related to the laser irradiation energy

The solidified films exhibit surface roughness, localized at the grain boundaries and formed due to density differentials between molten and solid silicon. As molten silicon solidifies, it expands. Crystal growth begins at seeds and the last molten material lies between growth fronts; when they collide, the newly solidified silicon can only expand upwards, resulting in protuberances associated with the grain boundaries formed. The resulting ELC polycrystalline silicon films are of much higher quality than furnace annealed SPC films. They exhibit much lower densities of intragrain defects, a factor much more important than the larger grain size also afforded by ELC. A disadvantage, however, is the difficulty of striking an optimum balance between film quality and uniformity. Furthermore, as the grain size in ELC films is comparable to TFT channel lengths, large statistical fluctuations due to grain boundaries may result. For short channel

lengths (e.g. <0.5 μm) we may have channels within a single grain, but the location of grain boundaries with respect to TFT channels would have to be precisely controlled. Several advanced ELC techniques have been proposed in recent years for optimum crystallization in order to tackle these issues [6].

The basic issue driving the development of advanced ELC techniques is the manipulation of the intrinsically unstable condition of superlateral growth in such a way as to allow for controllable engineering of the final film microstructure. In this sense, all these techniques can be grouped under the term "controlled SLG" (C-SLG). By controlling the shape and dimensions of areas being melted via several optical, photolithographic and other methods, C-SLG techniques can tailor the resulting film microstructure so as to yield controlled, predictable and uniform grain size and structure. This is a direct result of the relationship between the distance of lateral growth and the width of the irradiated area. The lateral growth distance is limited by the onset of nucleation inside the molten material or by the collisions of crystallization fronts growing from opposite sides of the molten area. By suitably selecting the width of the molten area formed by the laser irradiation in relation to the lateral growth distance nucleation events can be severely suppressed (Fig. 2). In this way, a very uniform film structure consisting of very elongated grains can be achieved over large areas [7]. Many techniques can be suitable for preselecting the areas that will be fully melted; these include silicon film thickness variation, coating of the a-Si film with a preformed antireflective film and projection shaping of the laser beam profile [8].

### 2.2. SLS ELA crystallization

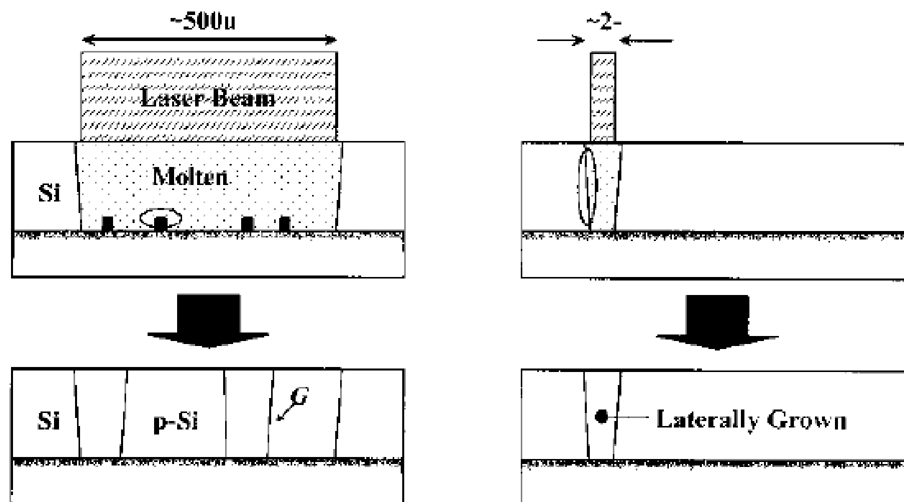


**Fig. 2** Superlateral growth (left) and controlled superlateral growth (right) of silicon crystals

One of the excimer laser annealing techniques that yields impressive results is sequential lateral solidification (SLS) [9]. In this technique laterally developed crystals (Fig. 2) can be elongated to vary large horizontal dimensions. This is accomplished by

shifting the sample in respect to the laser beam or shifting the beam in respect to the sample. If the shifting distance is shorter than the distance of superlateral growth, the Si film can be re-molten in such a way that the molten region is in contact to a part of the laterally developed grains from the previous step. This technique gives vary large grains of excellent intragrain quality (comparable to silicon on insulator-SOI), allowing the fabrication of devices within each of these optimum quality grains. By implementing the channel region within the high-quality crystallite, we avoid including in the channel region grain boundaries, which cause electron and hole energy barriers (Fig. 3) that are responsible for lower effective mobility values in transistors [10].

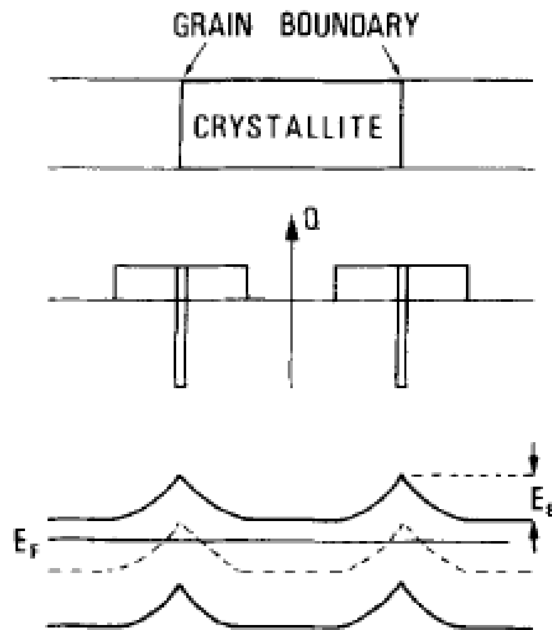


**Fig. 3** Effect of grain boundaries in the silicon energy diagram

## 3. Experimental

Since SLS ELA Si quality depends in the shifting of the sample in respect to the laser beam, several techniques can be employed in this direction, resulting in different crystal arrangements, crystallite dimensions and geometry. Scanning electron microscopy (SEM) images of the resulting films for each technique can reveal these characteristics, subsequently related to the electrical performance of the devices fabricated in them.

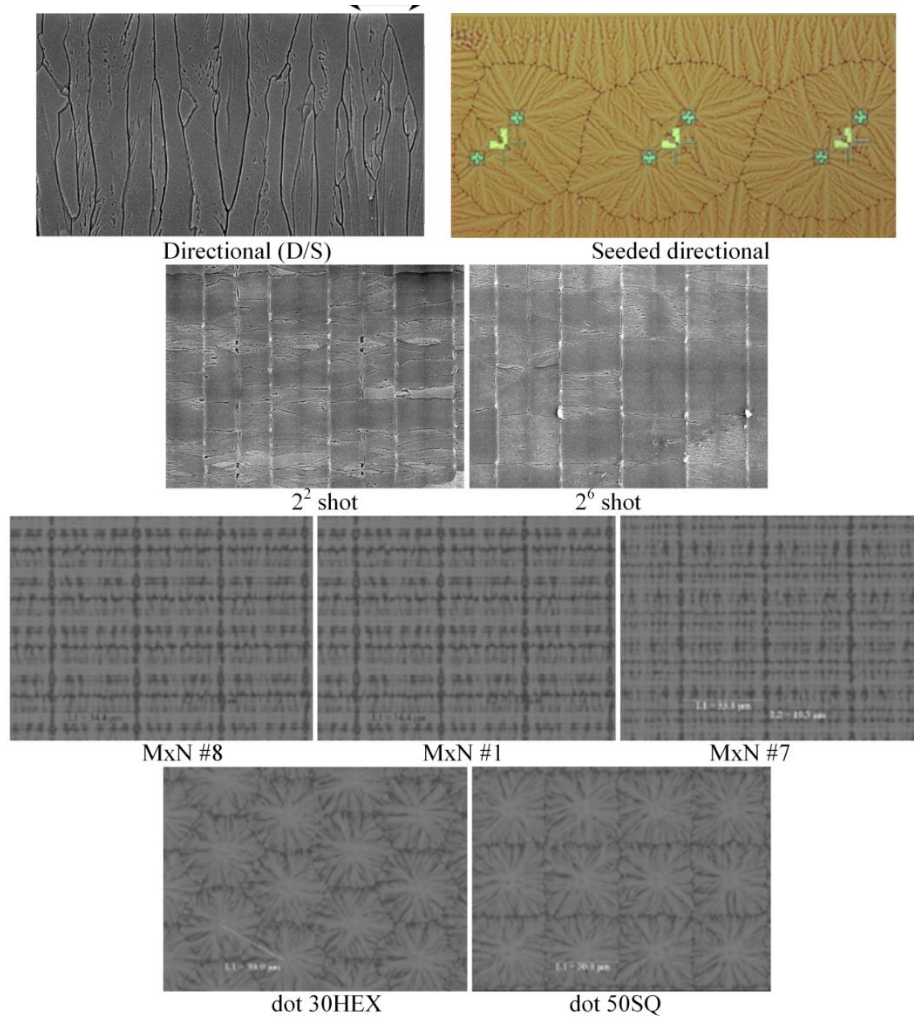


**Fig. 4** SEM images of the differently crystallized polysilicon films

In Fig. 4 we can see SEM images of the SLS ELA polysilicon films to be studied: directional [11], seeded directional [12], $2^2$-shot [13], $2^6$-shot [13], M×N shot [13] of different crystal dimensions, dot hexagonal and square crystallization [13]. All these techniques vary in the shape of the laser mask used with all other process parameters kept to the optimized values (i.e. room temperature, excimer laser wavelength, frequency etc). In directional crystallization films are crystallized with the laser beam shaped through a one rectangular slit (25μm wide). This rectangular laser beam melts the film locally and is then shifted to melt the adjacent region. In this way the whole film area is scanned, resulting in a film of many elongated and roughly parallel grains. In the seeded version, the laser mask is the same, but within the original film there are some crystal seeds at specific points, acting as the crystallization onsets. The result is radial grain boundaries,

following the crystal structure of the original seed. In the 2-shot technique the laser mask consists of two columns with parallel slits, slightly offset with each other. For $2^N$-shot techniques (in our case N = 2 or 6) the laser beam is split in a number of regions, each consisting of parallel slit sets, vertical to each other. Half of the N regions are x oriented and the other half are y oriented, again slightly offset with each other. The M×N technique is a variation of the previous one, with M slits in the x direction and N slits in the y direction.

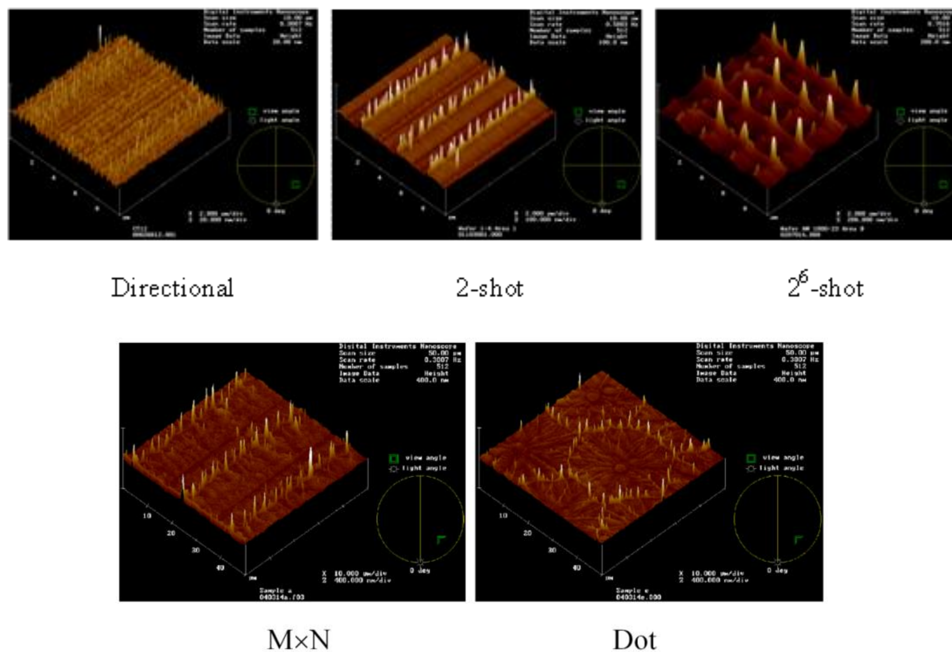


**Fig. 5** AFM images of the SLS ELA crystallized samples studied

Apart from the slit approach for shaping the laser mask, there is also the approach of dot array masks of appropriate geometry. In this case crystallization begins from the dot points and proceeds radially. The distance and geometry of the dots now defines the microstructure of the crystallized polysilicon. In our case, when the dots are arranged in a square array we form squarer grains and when they are arranged in a hexagonal array we get hexagonal grains.

In order to see the effect of crystallization techniques in the surface roughness of the films, we also characterized them through atomic force microscopy (AFM) [14], as presented in Fig. 5. As we can see, the larger the shot number in a film the larger the polysilicon protrusions observed and the larger the film surface roughness. Also, for M×N and dot crystallized films, where the intragrain quality is lower due to the sub-boundaries present (see SEM images of Fig. 4), film protrusions are more sparse and located mainly in the grain boundaries.

After the morphological characterization of the differently crystallized polysilicon films, TFTs were fabricated in them. We fabricated top gate [12], bottom gate [12] and double gate [15] devices, oriented in both the x and y direction of the films, since we saw that grains and grain boundaries are different with respect to the film orientation. The top gate insulator was a 30 nm thick PECVD $SiO_2$ and the bottom gate insulator was a 50 nm thick PECVD $SiO_2$. Different channel widths W and lengths L were studied, ranging from W = 1 μm – 100 μm and L = 0.5 μm – 4 μm.

The $I_d$ – $V_g$ TFT transfer characteristics were measured, utilizing a HP4140B semiconductor analyzer and a Keithley voltage source in a dark box under no illumination, in the linear region, with $V_d$ = 0.1 V. For the double gate TFTs, their transfer characteristics were recorded varying the bottom gate bias $V_{gb}$ from –3 V to 3 V. The maximum of the slope of the $I_d$ – $V_g$ characteristic, drawn in linear scale, yields the maximum transconductance $G_{m,max}$ at a particular gate bias $V_{g,max}$. The intercept, with the horizontal axis, of a straight line with that slope, fitted to the characteristic at $V_{g,max}$ yielded the extrapolated threshold voltage $V_{th}$. Also, the subthreshold slope for all measured devices was calculated.

For the degradation studies we conducted, the TFT structures were dc stressed, biasing appropriately the gate(s) and drain for a predefined stress time for each step, according to the stress condition selected for each experiment (see following paragraphs for details). After each cycle the $I_d$ – $V_g$ characteristics were measured in the linear region with $V_{ds}$ = 0.1 V and their electrical parameters ($V_{th}$, $G_{m,max}$ and S) were calculated.

## 4. RESULTS & DISCUSSION

### 4.1. Characterization Results

#### *4.1.1. Crystallization effects on TFT electrical parameters*

In Table 1 [13] we can see the average values of the threshold voltage $V_{th}$, the field-effect mobility μ and the subthreshold slope S of the measured TFTs. We examined two different variations of the Dot technology and three different variations of the M×N one, the only differences being (i) for the Dot technologies, the hexagonal dot matrix for the 30HEX samples vs. the square dot matrix for 50SQ ones, and (ii) for the M×N technologies, the crystal domain size.

As far as S is concerned, we can see that it appears to be increased for the samples having an increased number of grain boundaries within the channel area , with the sole exception of the Dot TFTs, where we would normally expect it to be higher, since it has the worst polycrystalline quality. This can be explained if we consider the effect of what kind of traps is reflected on each parameter. We know that through S midgap traps, mainly located in intragrain areas, can be probed. Therefore, the small S value of the Dot TFTs, considering the rather increased number of grain boundaries, can be attributed to more tail-states existing for that technology than midgap ones.

So, comparing the mean μ value of the TFTs crystallized with different technologies, we can see that the largest mobility values, approaching the single-crystalline reference one of SIMOX, are obtained for M×N TFTs, followed closely by 2-shot TFTs and then by $2^6$-shot and Dot ones. This order of these different technologies with decreasing mobility can be attributed to two factors: the grain-boundary trap density and the surface

roughness, causing more pronounced carrier surface scattering and therefore degrading device field effect mobility.

Considering these two factors, we see that the M×N TFTs, having the largest mobility values, indeed have the fewer grain boundaries of all and, at the same time, the less pronounced surface roughness. The next lowest value of grain boundaries is that for the $2^6$-shot sample, showing its very good polysilicon quality, also observed from the SEM image. Nevertheless, its mobility is lower than that of the 2-shot sample, having a similar crystal structure. This is because of the extremely pronounced roughness observed in the $2^6$-shot sample, as compared to the 2-shot one. Finally, the Dot TFTs having the largest number of grain boundaries, despite their small surface roughness, exhibit the smallest mobilities of all devices. Therefore, low grain boundary densities within the channel area are essential to obtain large field-effect mobility, but the effect of surface roughness should not be neglected, since it can substantially degrade the performance of a TFT.

**Table 1** Device parameter statistics for different crystallization techniques

| | | $V_{th}$ (V) | | μ ($cm^2$/V·sec) | | S (mV/decade) | |
|---|---|---|---|---|---|---|---|
| | | MEAN | STD | MEAN | STD | MEAN | STD |
| SIMOX | | -0.57 | 0.46 | 322.15 | 42.92 | 0.11 | 0.01 |
| 2-shot | | -1.87 | 0.56 | 282.31 | 67.02 | 0.39 | 0.25 |
| $2^6$-shot | | 0.21 | 0.23 | 187.33 | 62.83 | 0.16 | 0.03 |
| Dot | 30HEX | -1.31 | 0.28 | 163.01 | 37.97 | 0.23 | 0.04 |
| | 50SQ | 0.62 | 0.37 | 198.14 | 18.99 | 0.21 | 0.02 |
| M×N | #1 | -1.03 | 0.38 | 235.40 | 55.23 | 0.17 | 0.03 |
| | #7 | -0.95 | 0.29 | 321.96 | 26.50 | 0.19 | 0.05 |
| | #8 | -0.20 | 0.48 | 289.08 | 36.03 | 0.15 | 0.02 |

*4.1.2. $V_{g,max} – V_{th}$ parameter importance*

After measuring the $I_d – V_g$ characteristics of our top gate TFTs, we extracted their field effect mobility μ and the threshold voltage $V_{th}$. We, also, calculated graphically (Fig. 6), the difference $V_{g,max} – V_{th}$ for each device [16]; $V_{g,max}$ is the value of the gate voltage at which the maximum transconductance is observed.

In table 2 we can see their values for 5 different TFTs. A comparison between TFTs with their channels oriented vertical to grain boundaries and parallel to them shows much lower μ values for the former (A vs B and E vs D), since the grain boundaries are known to reduce the carrier mobility. However, $V_{th}$ does not seem to be as affected just by the channel orientation (A vs B and E vs D). Other technological parameters, such as oxide trapped charges and interface charges, are known to affect the $V_{th}$ value in a more pronounced manner. Observing the third parameter $V_{g,max} – V_{th}$ of the table, we see that its value is also not as strongly dependent on channel orientation as the carrier field effect mobility $\mu_{fe}$ (A vs B). Nevertheless, this parameter does not seem to follow exactly the same behavior as $V_{th}$ (C vs D and D vs E). Also, we see that while devices B, C and D have decreasing $\mu_{fe}$ the same pattern is not followed by the parameter $V_{g,max} – V_{th}$ although theoretically both parameters depend on poly-Si traps. However, it is known that the field effect mobility is strongly dependent on the lateral field distribution and therefore reflects more factors than $V_{g,max} – V_{th}$ (a parameter "seeing" the device on the verti-

cal electrical field direction), such as channel orientation with respect to the grain boundaries and surface scattering of carriers.

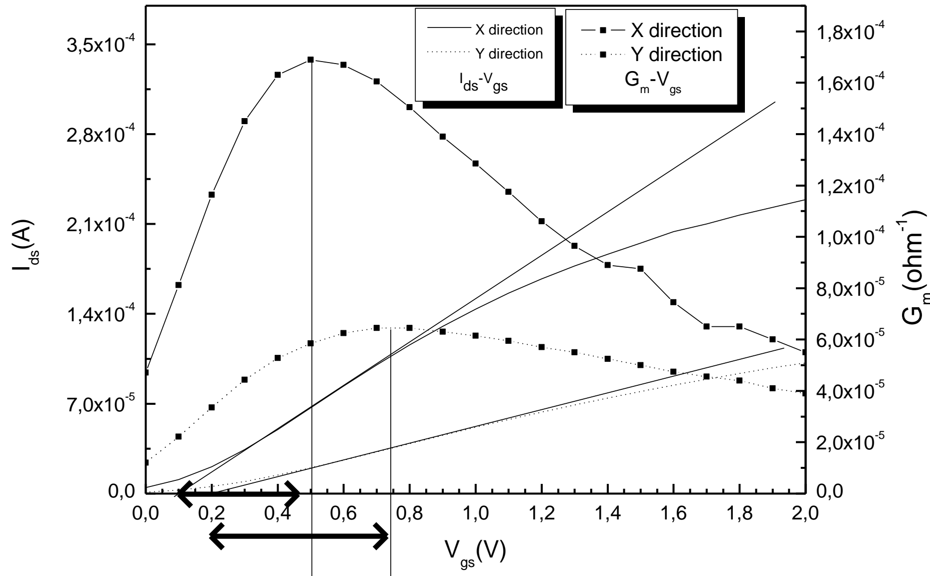


**Fig. 6** Graphic representation of the difference of the extrapolated threshold voltage $V_{th}$ and the voltage bias for maximum transconductance $V_{g,max}$ ($V_{g,max} - V_{th}$)

**Table 2** LTPS TFT electrical parameters

| TFT name | Grains vs channel | Field effect mobility $\mu_{fe}$ ($cm^2/V \cdot sec$) | $V_{th}$ (V) | $V_{g,max} - V_{th}$ (V) |
|---|---|---|---|---|
| A | ⊥ | 38 | 0.22 | 0.48 |
| B | // | 145 | 0.24 | 0.46 |
| C | // | 137 | 0.53 | 0.57 |
| D | // | 101 | 0.93 | 0.57 |
| E | ⊥ | 31 | 0.94 | 1.26 |

Therefore, from our previous analysis, we could say that the three studied electrical parameters seem to be independent from each other, each one reflecting different technological parameters: $V_{th}$ is known to reflect mostly interface traps and oxide charges, while $G_{m,max}$ (and $\mu_{fe}$) reflects polysilicon traps obstructing the current flow and scattering of the current carriers; $V_{g,max} - V_{th}$ reflects polysilicon traps irrespective of their effect on drain current, and specifically tail states, if we consider traps distributed within the band gap.

*4.1.3. Grain boundary effects on TFT performance*

We extracted the parameters and characteristics of single-shot and overlapping directional TFTs, oriented in the preferential (X) or the non-preferential (Y) direction [11].

Fig. 7 shows a schematic of the polysilicon structure in each case, with solid lines denoting hard grain boundaries and dashed lines soft ones, possibly due to extended defects. However, in addition to the boundary structure the two SLS variations exhibit another difference: in the overlapping irradiation case, due to the higher thermal load, coupled with the fact that the topography is usually not planar, the film exhibits much more pronounced roughness compared to the single shot case.

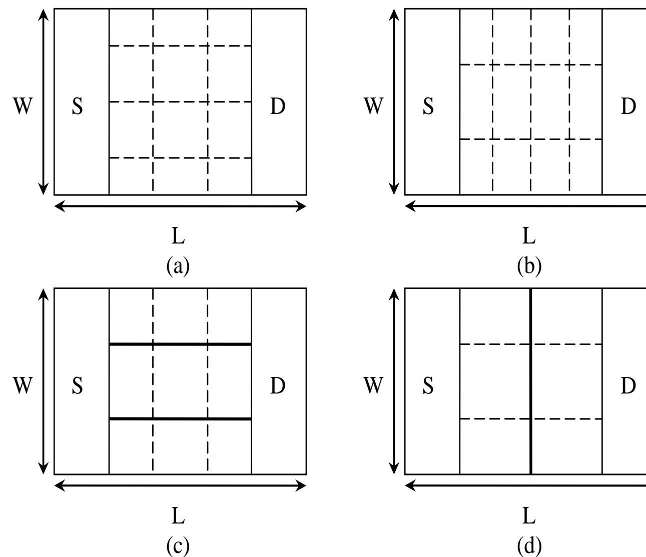


**Fig. 7** Rough schematic of grain boundaries for the overlapping directional sample in the preferential X (a) and the non-preferential Y (b) direction and for the single-shot sample in the X (c) and the Y (d) direction

Table 3 summarizes the electrical parameters of several devices from each technique. As can be seen for single shot devices, in the X-directed devices the mobility is four times higher than in the Y-directed one. If we consider the schematic of the grain boundaries in the X and Y directions (Fig. 7), we can see that in the X direction there are virtually no grain boundaries vertical to the current flow, explaining the large values of the mobility μ, while in the Y direction, where we observe very small mobility values, hard grain boundaries vertical to the channel exist.

Overall, the highest electron mobility is exhibited by single-shot X-direction TFTs, which have no vertical hard grain boundaries and no roughness. They are followed by overlapping irradiation TFTs of both orientations, which have no hard boundaries but have surface roughness and finally by single-shot Y-direction TFTs that usually have hard boundaries. The mobility is thus limited mostly by the presence of hard boundaries, but is also affected by surface roughness and to lesser degree by channel doping.

As we can see from Fig. 7(a) and 7(b), the Y direction for the overlapping irradiation sample is similar with the X direction, with no hard boundaries in either one; moreover, the presence of surface roughness in both cases tends to smear any directionality. That is why we observe almost the same behavior for both directions. The erratic values obtained

for small TFTs may be related to effects of roughness; moreover, for small dimension TFTs, there is a possibility for the channel to lie completely in the intragrain region, thus yielding very large mobilities. This behavior is not observed in narrow-width single-shot TFTs, which do not show surface roughness variations.

**Table 3** Average value and standard deviation of TFT electrical parameters for single shot and overlapping shots directional crystallization techniques, for both channel orientations

| | | $V_{th}$ (V) | | μ ($cm^2/V{\cdot}sec$) | | S (V/decade) | | $V_{g,max} - V_{th}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|
| Poly-Si | Direction | $\bar{x}$ | $\sigma$ | $\bar{x}$ | $\sigma$ | $\bar{x}$ | $\sigma$ | $\bar{x}$ | $\sigma$ |
| Single shot | X | 0,21 | 0,12 | 130,38 | 29,56 | 0,11 | 0,01 | 0,45 | 0,09 |
| | Y | 0,54 | 0,51 | 30,16 | 16,39 | 0,15 | 0,03 | 1,16 | 0,92 |
| Overlapping shots | X | 0,10 | 0,48 | 95,69 | 39,90 | 0,13 | 0,03 | 0,78 | 0,36 |
| | Y | 0,10 | 0,40 | 99,12 | 45,23 | 0,13 | 0,02 | 0,95 | 0,42 |

*4.1.4. Channel geometry effects*

Most of the previous studies [17, 18] in narrow-width effects on TFTs have shown a decrease of the threshold voltage with decreasing channel width (reverse narrow channel effect, i.e. opposite trend to the crystalline MOSFET narrow-width effect, which causes $V_{th}$ increase with decreasing channel width). However, all of the TFTs studied were in small-grain polysilicon with significantly larger trap densities. Only Yaung et al [19] reported a $V_{th}$ increase with decreasing channel width for hydrogenated polysilicon TFTs, where the trap density is reduced.

Typical $I_{DS} - V_{GS}$ characteristics [11] for different channel widths can be seen in Fig. 8 (directional crystallization). Both technologies of our TFTs, in both X and Y directions, exhibit a MOSFET-like behavior (increase of threshold voltage with decreasing channel width). This trend is more prominent in the Y-direction for the single-shot TFTs, while for the overlapping irradiation case devices of both directions exhibit the same behavior.

The narrow-width effects are more prominent on the threshold voltage of the transistors than on their electron mobilities.

It is believed that this narrow-width effect is caused by the increased trap or charge density at the edges of the polysilicon or the oxide, respectively (possibly caused by the etching of the polysilicon islands and the gate oxide and the following $n^+$ implantation), causing a depletion region at the channel edges. These edge effects can be ignored for large channel widths, but become significant when the width is reduced and the charge or trap induced depletion regions are comparable to the channel width.

Observing the $I_{DS}$-$V_{GS}$ curves (Fig. 8) for transistors of the same length and several widths, we notice that they exhibit a parallel translation, i.e. a flatband voltage shift that is attributed to the depletion regions at the channel edges. We also observed a, less obvious, increase in the trap density $D_{ts}$ with decreasing channel width, leading us to the conclusion that the trap density at the edges is also larger than that for the rest of the film, since the edge effects become important for small widths.

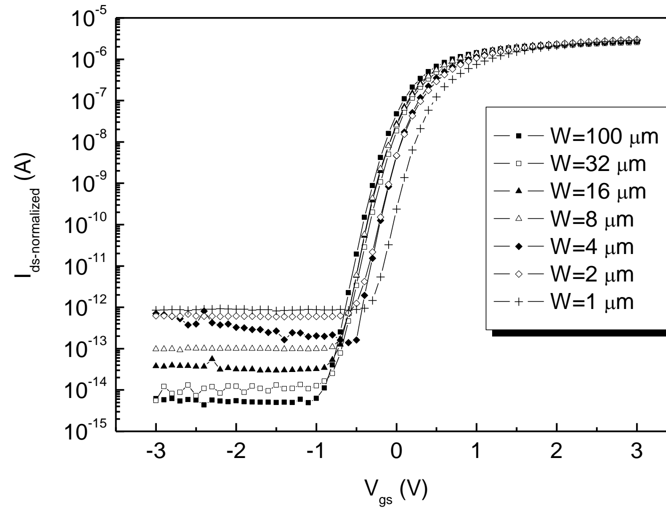


**Fig. 8** Normalized $I_{DS}$-$V_{GS}$ characteristics for several channel widths of TFTs with channel length L = 1 μm, for single-shot devices oriented in the preferential direction

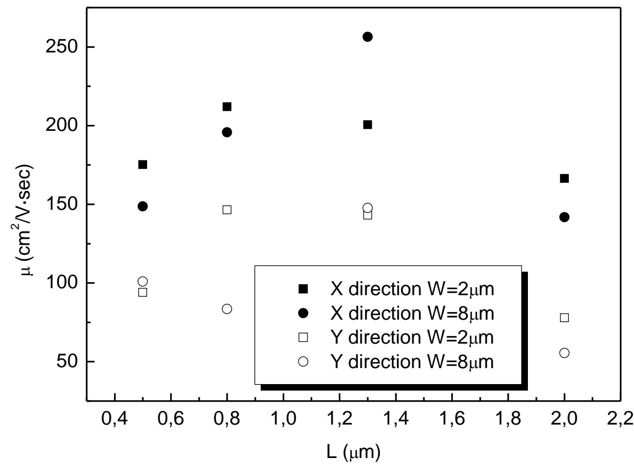


**Fig. 9** Field-effect mobility μ as a function of channel length L for M×N crystallized SLS ELA TFTs

As far as the channel length is concerned, in Fig. 9 we can clearly see that the field effect mobility of all of the X oriented devices (M×N crystallization) is significantly larger than that of the Y oriented devices, which supports the DLTS conclusion that in the preferential X direction the process results in better intragrain quality due to "softer" sub-boundaries [20]. For larger or smaller channel lengths than 1.2 μm the performance seems to deteriorate. This optimum length addressing to intermediate L values shows enhanced performance and could be related to the subthreshold slope S of the devices

[20]. The increasing mobility with increasing L, in the L regime below 1.2 μm, is something expected, since, observing the SEM image, we see that more sub-boundaries are included within the channel region for longer channel lengths. The increase of S with decreasing channel length, in the L regime above 1.2 μm, is an electrical effect, ascribed to the increased channel charge in the subthreshold regime due to the additional drain bias control of the channel region. So the deterioration of the TFT performance for small channel lengths is an electrical effect while the deterioration for large channel lengths is process related. These two mechanisms define the optimum channel length.

*4.1.5. Top, bottom and double gate TFT structures*

We also tried to see if the device structure has any effect on their electrical performance. For this reason we measured several top and bottom gate devices seed crystallized and extracted their electrical parameters' mean value and standard deviation (Fig. 10). As we can clearly see, for the preferential direction (Y in this case), featuring less sub-boundary traps, the mobility values are significantly lower for bottom gate devices, attributed mainly to the much worse interface trap density of the bottom oxide [21]. Also, for p-channel devices we observed a less intense directionality effect and lower standard deviation in mobility values, probably due to the effect of dopant segregation in the areas of the grain boundaries [22].

We proceeded in the investigation of short channel effects characterizing p-channel TFTs crystallized with the seed location control technique. As we can see in Table 4, there is a significant effect of channel doping on this poly-Si film quality, since the difference $V_{g,max} - V_{th}$ (which is proportional to the density of poly-Si traps) of p-TFTs is significantly smaller. This could insinuate that there are fewer poly-Si traps in p-channel devices, probably due to the lack of doping segregation after p-type doping, thus not increasing the grain boundary energy barrier as much as in n-channel TFTs.

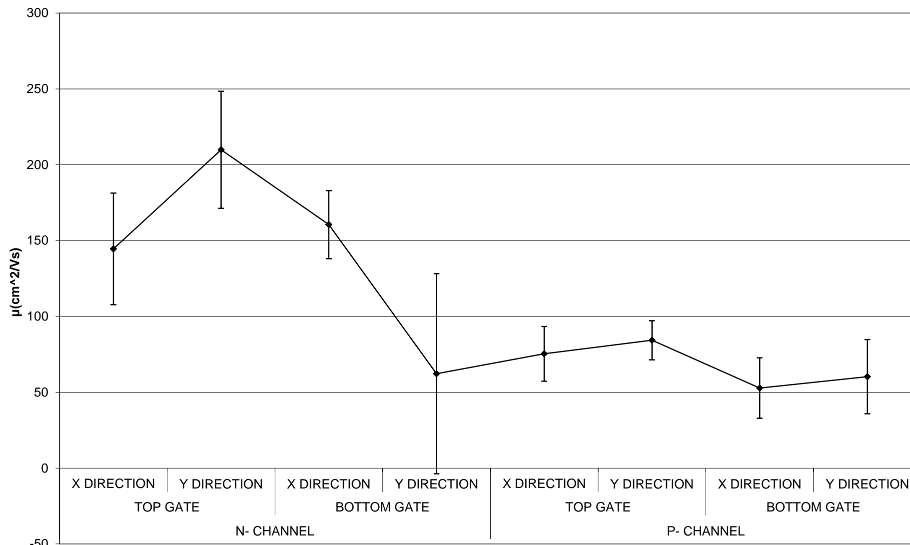


**Fig. 10** Field-effect mobility μ mean values and standard deviation for seed crystallized SLS ELA TFTs n- and p- channel, top and bottom gate, X and Y direction

**Table 4** Mean electrical parameter values for seed location control technique n- and p- channel TFTs

| | $V_{th}$ (V) | | μ ($cm^2$/V·sec) | | S (V/decade) | | $V_{g,max} - V_{th}$ (V) | |
|---|---|---|---|---|---|---|---|---|
| Direction | n- | p- | n- | p- | n- | p- | n- | p- |
| X | 0,78 | -0,99 | 144,51 | 75,38 | 0,14 | 0,12 | 1,59 | 0,85 |
| Y | 0,35 | -0,86 | 209,85 | 84,30 | 0,13 | 0,12 | 1,17 | 0,85 |

Following that, we characterized double gate devices with a structure schematically shown in Fig. 11, fabricated with the same process as the single gate devices previously analysed. While varying their bottom gate bias as a parameter, we recorded their transfer characteristics $I_d - V_{gt}$ for top gate operation, as shown in Fig. 12. It is evident that there is a continuous shift of the $I_d - V_{gt}$ characteristic for changing $V_{gb}$ value, indicating a continuous back gate effect and strongly suggesting that the device is fully depleted at all conditions. The device parameters ($V_{th}$, S, $G_{m,max}$), as measured for front gate operation, were observed to depend on $V_{gb}$ in a manner reflecting the varying back channel contribution, with a confluence of $V_{th}$ and S values for varying $V_{gb}$. However, the use of the back gate was determined to offer linear threshold voltage control, thus allowing for enhanced flexibility in TFT circuit design. Moreover, the application of back gate bias makes possible the significant reduction, for similar drain current levels, of the avalanche effect observed at high drain voltage values, as compared to the case when only a front gate bias is applied [15].

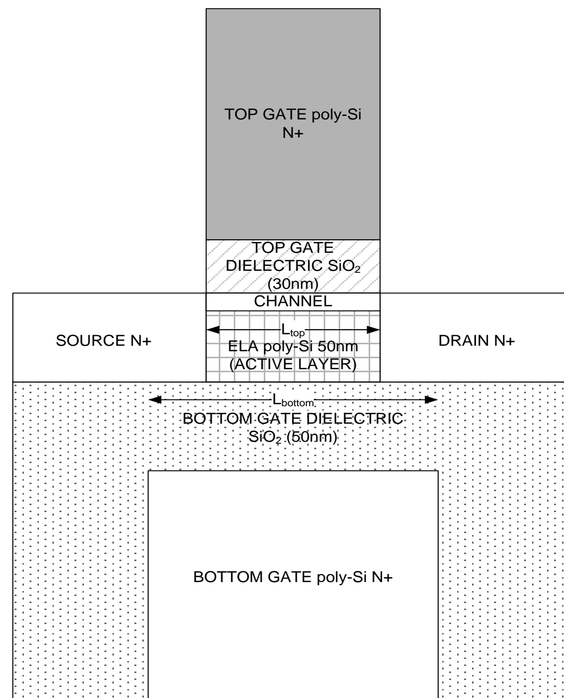


**Fig. 11** Schematic of double gate TFT structure

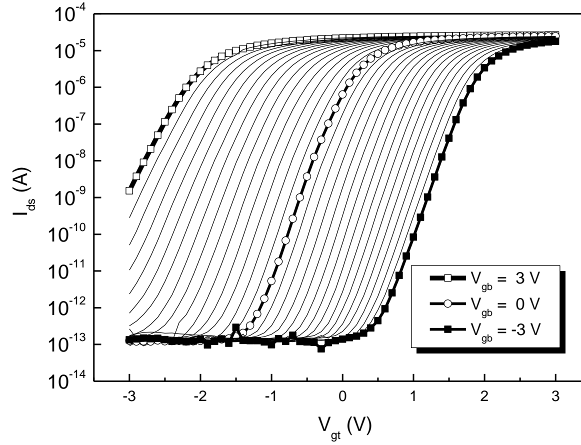


**Fig. 12** $I_d$-$V_{gt}$ characteristics for front gate operation of a double gate (DG) TFT, with the back gate bias $V_{gb}$ as parameter

## 4.2. Degradation results

### *4.2.1. Channel type and direction effects on degradation*

In order to investigate the reliability differences between n-channel and p-channel devices of the same dimensions (W/L = 2μm/2μm), we applied analogous stress biases for $V_{gs}$ and $V_{ds}$, utilizing the stress condition $V_{gstress} = V_{dstress}/2$, as mentioned before [23]. For the n-channel devices the stress biases used were $V_{gstress}$ = 4V, $V_{dstress}$ = 8V [20]. The analogous stress biases used for p-channel devices, observing that their absolute $V_{th}$ value was about 1V higher than the n-channel ones, were $V_{gstress}$ = −5V, $V_{dstress}$ = −10V.

In Fig. 13 we see the evolution of the extrapolated threshold voltage $V_{th}$ for both n-channel and p-channel devices, oriented both along the preferential X and the non-preferential Y direction. For the n-channel devices we see a large difference between the two orientations. For the p-channel devices, on the other hand, the two channel orientations show similar behavior. The largest $V_{th}$ degradation is observed for the X oriented n-channel device, that has the largest carrier mobility of all the investigated devices [20].

As for the subthreshold slope S of the devices (Fig. 14), the only device showing an increase is again the X oriented n-channel TFT. All the other devices show almost no S variation, indicating insignificant interface state generation.

The previous observation that for the p-channel devices the channel orientation plays a smaller role is further supported considering their mobility values (Fig. 15). While for n-channel devices the X direction mobility is approximately double in value than the Y one, the p-channel X direction mobility is only about 10% higher than the Y one. Also, both p-channel devices show similar μ degradation, with a slight increase for large stressing times, indicating a minor channel shortening effect. This behavior is much different than that of n-channel TFTs, for which the Y direction shows no degradation at all, but the X direction shows an initial, much swifter channel shortening effect, followed by a large decrease.

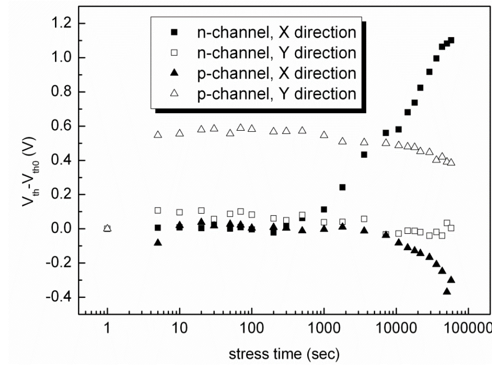


**Fig. 13** Evolution of extrapolated threshold voltage $V_{th}$-$V_{th0}$ with stress time for both n- and p-channel devices under analogous stress conditions

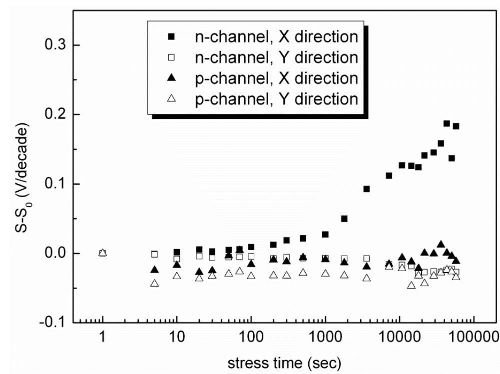


**Fig. 14** Evolution of subthreshold slope S-$S_0$ with stress time for both n- and p-channel devices under analogous stress conditions

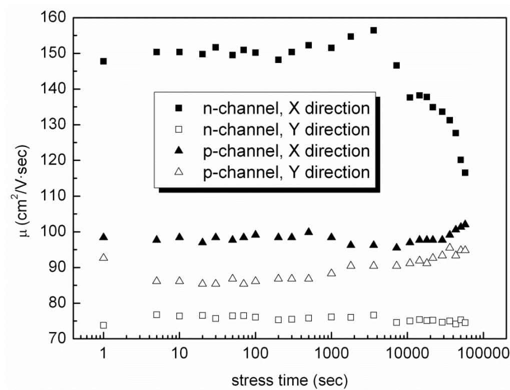


**Fig. 15** Evolution of field effect mobility μ with stress time for both n- and p-channel devices under analogous stress conditions

*4.2.2. Effects of polysilicon film thickness on degradation mechanisms*

For directional SLS ELA TFTs with channels oriented along the elongated grains the variation of degradation mechanisms for increasing polysilicon active layer thickness was investigated [24]. Fig. 16 shows the degradation of the maximum transconductance ($G_m$) and threshold voltage ($V_{th}$), as a function of film thickness and stress time at $V_{GS}$ = 7 V. It has been suggested that both $G_m$ and $V_{th}$ time-dependent degradation, under bias stress can be empirically modelled by a power law [24-26]:

$$\Delta = C \cdot t^n \tag{1}$$

where "$\Delta$" is $\Delta G_m = |G_{m,o}-G_m|/G_{m,o}$ or $\Delta V_{th} = |V_{th,o}-V_{th}|$, "$C$" is a pre-factor, "$t$" is the stressing time and "$n$" is the power-law exponent. The power-law exponent has been previously connected to the degradation mechanism, particularly for $V_{th}$ shifts. Power-law exponents in the range of 0.1-0.3 for bias-stress-induced $V_{th}$ shifts in poly-Si TFTs indicate hot-carrier injection, whereas exponents of 0.4-0.6 indicate deep-state generation, presumably at crystal-domain boundaries [26-29]. We have investigated the power-law fits of $V_{th}$ and $G_m$ degradation in directional SLS ELA TFTs and extracted the exponent "$n$" values as a function of film thickness and gate-bias stressing voltage; they are plotted in Fig. 17.

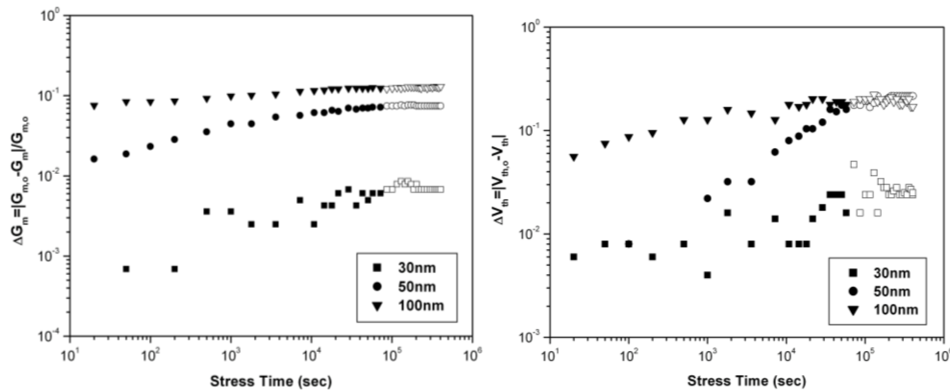


**Fig. 16**`Degradation in $G_m$ (left) and $V_{th}$ (right) as a function of poly-Si active layer thickness and stressing time at $V_{GS}$ = 7V, $V_{DS}$ = 14V. We note that only the data ranges represented by the "filled" symbols (for each thickness) were used to extract the power-law exponents shown in figure 2 for $\Delta G_m$ and $\Delta V_{th}$

For TFTs with 30 nm thick active layer the observed $G_m$ degradation is primarily attributed to carrier trapping at defect sites [29]. The poly-Si film crystal quality improves with thickness increase to 50 nm and 100 nm, evidenced by the development of wider crystal domains and a reduced trap density in the sub-boundary regions [30]; thus, the $G_m$ degradation rate decreases with film thickness. This is reflected in the declining trend in the power-law exponent with the active-layer thickness, shown in Fig. 17. However, the $V_{th}$ degradation power-law dependence yields exponent values exhibiting a non-monotonic trend with film thickness. For the thinnest value (30 nm) the $V_{th}$ degradation mechanism is consistent with hot-carrier injection into the gate insulator layer. For devices

with 50 nm thick active layer, it is more consistent with the generation of deep trapping states at grain boundaries. For the case of 100 nm TFTs, the degradation mechanism reverts back to injection and trapping of hot carriers.

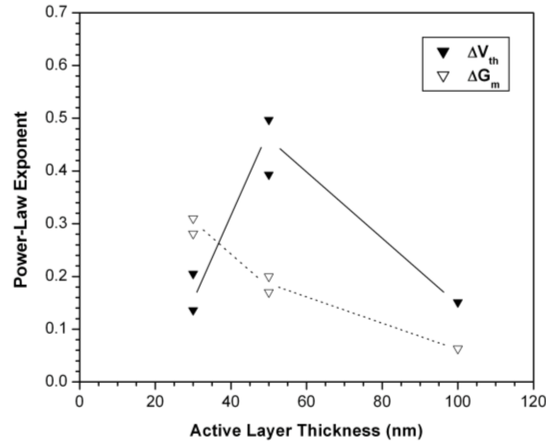


**Fig. 17** Extracted power-law exponent for $G_m$ and $V_{th}$ degradation as a function of the polysilicon active layer thickness (bias stress at $V_{GS}$ = 7 V and $V_{DS}$ = 14 V)

We have proposed an explanation based on the combination of a vertical built-up field and partial depletion to account for this $V_{th}$ degradation behavior [24]. Assuming that trap sites are neutral when unfilled and appropriately charged when filled with majority carriers, electron trapping will result in the buildup of a field within the active layer, with a direction pushing electrons towards the oxide, producing the same effect on non-trapped electrons as the vertical field exerted by the positive gate bias. In ultra-thin active layer TFTs, carrier trapping has been established as the main $G_m$ degradation mechanism. This results in a vertical electric field enhancement, assisting hot-electron injection towards the gate insulator layer. This is consistent with the observed trend in $V_{th}$ degradation in TFTs featuring 30 nm-thick active layer. When the active layer thickness increases to 50 nm, the $G_m$ degradation rate decreases and the effect of carrier trapping is weaker, which is directly related to the better crystal quality of thicker films. No sufficient enhancement in the vertical field occurs and the main mechanism for threshold voltage degradation is the formation of deep states, most likely at domain sub-boundaries, judging by the associated exponent value [6]. This mechanism, new state formation, agrees with the increase in the grain boundary trap density observed in 50 nm thick active layer TFTs, compared to 30 nm thick ones, as shown in Fig. 18, where the Levinson-extracted grain boundary trap density [31] is plotted against stress time for various film thicknesses. We note the rapid trap density increase for 50 nm-thick TFTs, in contrast to the nearly flat line for 30 nm-thick ones. We also observe that much of the degradation for 100 nm TFTs occurs in a short initial interval, probably due to higher material quality that allows faster carrier heating; after the first 20 sec of stressing, and up to $10^4$ sec, the rate of trap density increase is even higher for TFTs in 50 nm thick films than in 100 nm thick films, while the rate is similar for large stress times. As for $V_{th}$ degradation, a non-monotonic variation of the degradation rate with film thickness is observed.

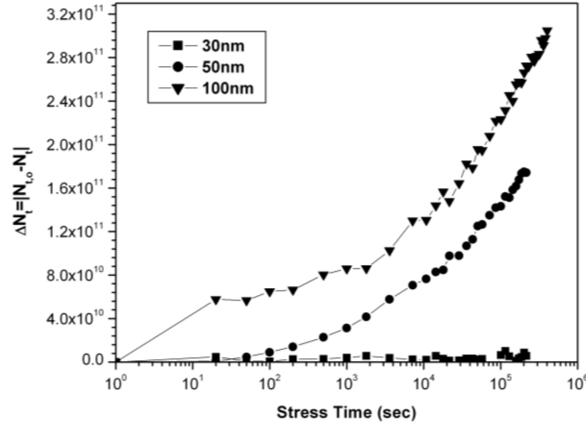


**Fig. 18** Grain boundary trap density $N_t$ evolution with stress time, for various active layer thicknesses. $N_{t,o}$ is the value of $N_t$ at t = 0 sec

For TFTs in the thicker 100 nm films the buildup of a negative field within the active layer is even less pronounced than for the 50 nm case. However, hot electron injection and trapping is again inferred, from the power law exponent, as for the 30 nm devices, to be the dominant degradation mechanism; the higher extracted exponent value, indicating a dominant mechanism of generation of deep trapping states at grain boundaries, is only observed in the 50 nm case. This is explained using the reasonable assumption that the 100 nm thick poly-Si film is only partially depleted, while the 30 nm and 50 nm thick ones are fully depleted. Actually, in SOI device studies a film thickness of 100 nm has been identified as the boundary between full depletion and partial depletion regimes [32]. As the defect density in polysilicon is higher than in single crystal SOI films, we expect this demarcation point to be shifted towards thinner active layer thickness. Thus, even though the bulk field due to filled traps, which enhances hot electron injection, for 100 nm thick TFTs is even lower than 50 nm ones, in the 100nm case many active layer electrons recombine in the neutral region at the bottom of the film and do not contribute to new sub-boundary state creation. That is, the partial depletion suppresses that mechanism for the thickest films.

### *4.2.3. Channel width effects on degradation*

Since channel dimensions are a critical parameter for high-performance devices, we tried to clarify the degradation mechanisms observed by varying the channel width. A DC hot-carrier stress ($V_{GS,stress}$, $V_{DS,stress}$) = (3 V, 6 V) was applied for durations up to 60 h; the $I_{DS} – V_{GS}$ curves were recorded at the conclusion of each stress cycle and the device parameters were extracted. In order to investigate the channel width dependence of stress-induced effects in polysilicon TFTs, we applied that same electrical stress condition in devices with various gate widths from 4 to 100 μm.

Fig. 19 shows the deviation of the initial threshold voltage $\Delta V_{th}$, extracted after each stress cycle for devices with different channel widths. We observe an increase of $\Delta V_{th}$ during stress time, which is a common behavior in all devices except for the narrower devices that exhibit an initial decrease and then an increase. The amplitude of positive $\Delta V_{th}$ shift scales up with width. Narrower devices (with W of 4 and 8 μm) demonstrate less

pronounced $\Delta V_{th}$ positive shift. Moreover, the onset of positive $V_{th}$ shift occurs at shorter stress durations for wider devices than for narrower ones and it starts progressively earlier with increasing width. We also witness two slopes in the $\Delta V_{th}$ vs. logarithmic stress duration plot for all devices except for the narrower ones. Beyond a transition point, which scales down with width, the $\Delta V_{th}$ vs. logarithmic stress duration curve exhibits a second slope, which seems to be width-independent and is of the same magnitude for all devices. On the contrary, the magnitude of the slope of each curve up to the above mentioned transition point, depends on width and is progressively larger for the wider devices [33].

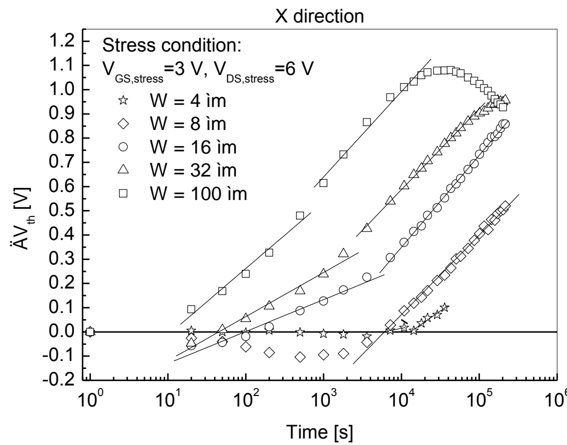


**Fig. 19** Threshold voltage variation during stress for X-directed polysilicon TFTs with various channel widths

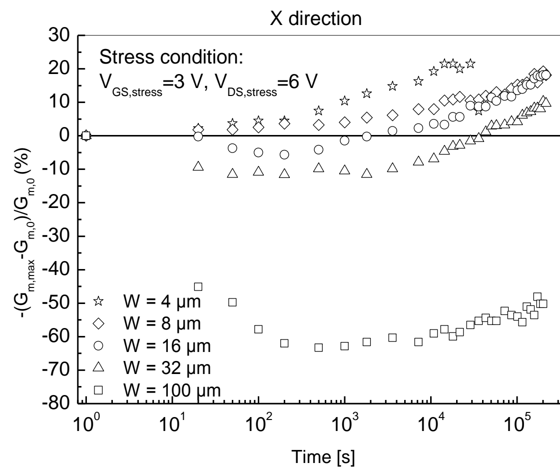


**Fig. 20** Percentage change of transconductance maximum vs. stress time for X-directed polysilicon TFTs

Fig. 20 shows the percentage change of the maximum of transconductance vs. stress time for X-directed TFTs. We observe that the devices with W = 16, 32 and 100 μm exhibit a similar behavior, which is an initial increase in $G_{m,max}$ (transconductance "over-

shoot") and then a reduction after reaching a maximum $G_{m,max}$ value. In the case of narrow devices (W = 4 and 8 μm), $G_{m,max}$ continuously decreases during stress and no "overshoot" is observed. Again, the initial increase of transconductance for wider devices scales up with width, whereas the later decrease is common and of the same magnitude for all the devices, independently of width. It is worth noticing that the transition point of stress duration, after which $G_{m,max}$ demonstrates a reduction from the maximum value, corresponds to the same transition point where the second slope in $\Delta V_{th}$ vs. log(t) curve (Fig. 19) appears for devices with W = 32 and 100 μm. We have to mention that for the narrowest device (W = 4 μm) only one slope in the $\Delta V_{th}$ vs. log(t) curve (Fig. 19) is detected and for the device with W = 8 μm the two slopes are slightly distinguished.

The difference in stress induced degradation behavior between narrow and wider devices reflects the fact that in the latter case the drain current is much larger, with less pronounced edge effects, and the electrons carrying it acquire larger energy, as self-heating effects are more pronounced; this increases the probability of hot electron injection. In the case of narrow TFTs this source of energy is not significant and hot holes are mainly responsible for the degradation, since they have larger effective mass and induce interface state generation, as inferred from the severe $G_{m,max}$ degradation [33].

#### *4.2.4. Short channel effects on LTPS TFT degradation*

The scope of our work in this field was to determine if there are any short channel effects present in the degradation of SLS ELA TFTs [34]. The investigated TFTs were n-channel double gate devices [15] with 50 nm polysilicon films that were formed by excimer-laser annealing of amorphous silicon, using the single-shot location control variation of the sequential lateral solidification (SLS) technique, preferentially oriented. The DG TFTs were dc stressed using a HP4140B semiconductor analyzer and a Keithley 230 voltage source. The transfer characteristics $I_{ds} - V_{gt}$ with respect to the top gate bias $V_{gt}$ for a back gate bias $V_{gb} = -3$ V, so as to ensure the conduction is mainly at the top interface, were measured in the linear region with $V_d = 0.1$ V after each stress cycle. To exclude effects from horizontal field variation, due to the different channel length, $V_{dstress}$ was scaled proportionally to $L_{top}$ for each device. The top gate stress bias was selected to be $V_{gtstress} = V_{th}(V_{gb} = -3\text{ V}) + 2$ V, while the bottom gate bias $V_{gbstress}$ was kept constant at -3 V, as stated before, pushing the carriers to the top interface.

We applied dc stress to double gate TFTs with different top gate length $L_{top}$, channel width of W = 8 μm and bottom gate length $L_{bottom} = 4$ μm. Observing the current-voltage characteristic curves after each stress cycle (Figs. 21-23) we saw that the degradation becomes much more intense for longer channels, although the horizontal electric field is exactly the same as for the shorter ones. We believe that this is attributed to the structure of the polysilicon film, since the longer the channel the more grain boundaries and sub-boundaries will be present. The more traps are present within the film the larger the degradation that will occur in the device, due to the extra trap state generation in these locations. We also observed two $V_{th}$ degradation mechanisms: hole injection observed only for large channels and electron injection common for all devices. From S evolution with dc stress we saw that these mechanisms mainly refer to trap generation at the interface and not oxide injection. As for $G_{m,max}$, we saw a similar behavior for all TFTs, featuring a monotonous decrease. This was attributed to grain boundary and sub-boundary trap generation, as indicated also by the $V_{g,max} - V_{th}$ evolution with stress time. The proposed degradation mechanisms are supported by low frequency noise measurements.

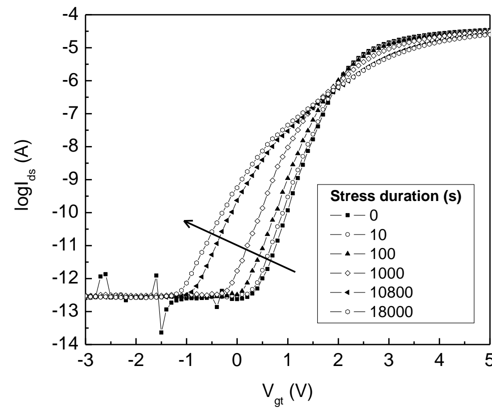


**Fig. 21** $I_d$-$V_{gt}$ curves after successive dc stress cycles for a DG TFT with $L_{top}$ = 0.5 μm

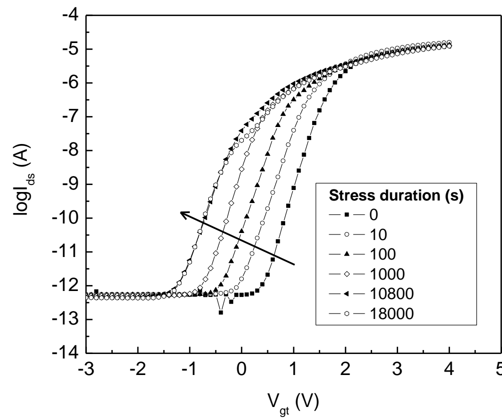


**Fig. 22** $I_d$-$V_{gt}$ curves after successive dc stress cycles for a DG TFT with $L_{top}$ = 0.8 μm

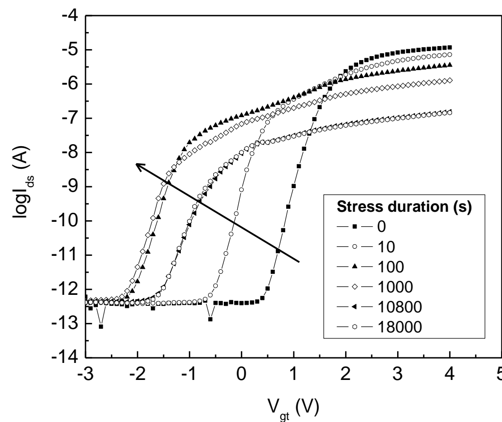


**Fig. 23** $I_d$-$V_{gt}$ curves after successive dc stress cycles for a DG TFT with $L_{top}$ = 1.3 μm

### *4.2.5. Degradation modeling*

One of the major issues associated with the high performance of polysilicon TFTs is their reliability when they are subjected to a high drain bias and a variety of gate bias voltages [26, 35, 36]. Due to the enhanced fields, mainly near the drain junction, the performance of TFTs is degraded, and their electrical parameters are shifted, leading to unpredictable circuit design failures when TFTs are used as circuit elements [37]. Our motivation for the following studies was to provide a simple and practical model that predicts the shift of the electrical parameters of polysilicon TFTs subjected to high stressing fields, both as a function of the stress regime (condition) and with regard to the scalability of the channel width. The width is an essential parameter for circuit designers, as in tapered (scaled) inverter chain complementary MOS circuits implemented using consecutive (cascade) inverter stages with W/L transistor ratios many times larger than those for previous stages [37]. Moreover, the operation conditions of TFTs used as circuit elements (as in cascode configurations [38]) are different for each device, resulting in electrical parameter shifts (compared to linear operation) and circuit design pitfalls that must be predicted and related to stress damage.

Even though hot-carrier phenomena have widely been studied in MOS poly-TFT structures [39], their quantitative [40] impact in the reliability and performance characteristics of poly-TFT devices of different channel widths after electrical stressing under different stressing conditions has been described only to a limited extent. Moreover, even in the models developed for the mature technology of silicon-on-insulator devices [41], typical bulk MOSFETs [42], and a-Si:H TFTs [43], the effect of subjecting devices with various channel widths under different hot-carrier stress conditions has not been analyzed, and mainly shallow trench isolation p-type MOS devices were examined [44]. Consequently, the effect of different hot-carrier stressing conditions on the 1-D current–voltage characteristics as a function of the channel width needed to be further examined.

The developed degradation model takes into account the formation of two regions, i.e., a defective region and a non-defective one, as presented elsewhere [42]. The equivalent circuit model [45] of a device subjected to the electrical stress is represented by two TFTs connected in series (Fig. 24).

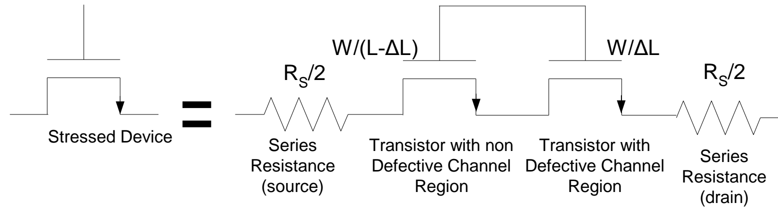


**Fig. 24** Schematic of TFT structure (left) and its equivalent electrical representation after electrical stressing (right). The developed model suggests the formation of two channel regions that are represented by two transistors connected in series

In order to obtain a simple and practical expression, so as to predict the hot-carrier damage for large-grain-size polysilicon TFTs, we use the ON-current model proposed in [46], i.e.,

$$I_D = \frac{W}{L} C_{ox}(V_G - V_{th})V_D \times \frac{\mu_G}{1+(\mu_G/\mu_{GB})(L_{GB}/L_G)\exp(qV_b/kT)} \times \frac{1}{1+\theta(V_G - V_{th})} \quad (2)$$

where $L_{GB}$ is the average grain boundary length, $L_G$ is the average intragrain length, $\mu_G$ is the intragrain mobility, and $\mu_{GB}$ is the grain boundary mobility. From (1), the effective mobility is given by

$$\mu_{eff} = \underbrace{\frac{\mu_G}{1+(\mu_G/\mu_{GB})(L_{GB}/L_G)\exp(qV_b/kT)}}_{\mu_0} \frac{1}{1+\theta(V_G - V_{th})} \tag{3}$$

The first term of the effective mobility expresses the effect of the grains and grain boundaries of polysilicon TFTs for low gate fields (low field mobility, denoted as $\mu_o$ in the text), and the second term expresses the first-order surface scattering effect on the mobility attenuation [47].

Assuming monoenergetic traps at the grain boundaries, the grain boundary potential barrier is gate voltage modulated and is given by the relation

$$V_b = \frac{t_{si}(qN_{tGB})^2}{8\varepsilon_{si}C_{ox}(V_G - V_{th})} \tag{4}$$

After theoretical calculations, utilizing the above mentioned assumptions [45] we obtain the model fitting function, i.e.,

$$\frac{g_m V_{DS} C_{ox}}{I_{DS}^2} = \left[ \frac{L}{W\mu_{0,nd}(V_{GS}-V_{th,nd})^2} - \frac{\Delta L}{W\mu_{0,nd}(V_{GS}-V_{th,nd})^2} + \frac{\Delta L}{W\mu_{0d}(V_{GS}-V_{th,d})^2} \right] \tag{5}$$

In the latter equation 4, the terms of the left-hand side are all determined by the measured data. The right-hand side is the fitting function that contains all the previously reported fitting parameters. By fitting the derived equation of the model to the experimental data, which correspond to the region $V_{GS} > V_{GS,peak}$, we obtained the parameters of the presented model. It should be noted that the parameters obtained from the fitting take their mean values.

We suggest that the degradation model predicts the maximum value of the threshold voltage of the two devices, corresponding to the two regions (defective and non-defective), connected in series in the equivalent circuit, which is expected to be the combined $V_{th}$ for two devices in series. If the degradation is uniform, the corresponding threshold voltage will be equal for the two regions, whereas if the damage is non-uniform (but more or less extended along the channel) the predicted threshold voltage of the whole device is, to a good approximation, that of the one at the defective channel region (which is the larger one). This approximation is supported theoretically [48]; in a non-uniform channel, with regions having different local threshold voltages each of which is considered as a separate device, the overall $V_{th}$ is the weighted $V_{th}$ over the channel (i.e., that of each device). However, as inversion in the defective channel part is harder to achieve, reflecting a much larger weight, the overall weighted threshold voltage is the average threshold voltage of the defective channel part. This is reasonable, as the threshold voltage reflects the mean concentration of free carriers and not how these carriers are transported between the source and the drain. The damage that occurs in the defective part of the channel region is reflected in two additional parameters: the defective region length ΔL, which is proportional to the interface state and/or the oxide trap state creation, and the mobility of charge carriers in the defective channel portion that depends on the defect charge density at the $Si/SiO_2$ interface and/or in the oxide.

Fig. 25 demonstrates the extracted threshold voltage shift (dot lines) and the overall threshold voltage shift predicted by the model (solid lines) for devices with different

widths subjected to the stress condition $V_{GS,stress} = V_{DS,stress}$. Indeed, our model seems to fit the experimental data very well. In Fig. 26, we observe the fitting results obtained from the application of the model, as concerns the critical parameter of the extent ΔL of the defective region. It is observed that the degradation is more pronounced in wider devices. The percentage variation of the length of the defective region predicted from the model gives reasonable values. It is found that ΔL stretches more slowly for narrower devices toward the source with a time dependence as follows: $\Delta L \propto t^n$, with $0.16 \leq n \leq 0.26$. For the device with W = 100 μm, ΔL obeys a saturation law.

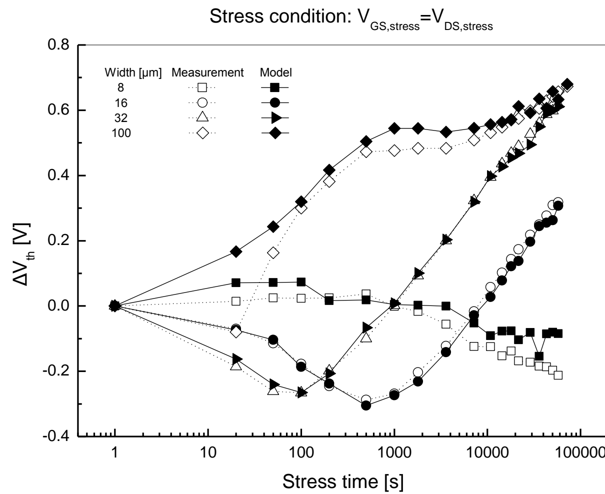


**Fig. 25** Threshold voltage variation for devices of various widths W = 8, 16, 32 and 100 μm and of a common length L = 0.8 μm. Stress condition: $V_{GS,stress} = V_{DS,stress}$. Extracted threshold voltage values (dot lines and open symbols) and those predicted by the model (solid lines and filled symbols)

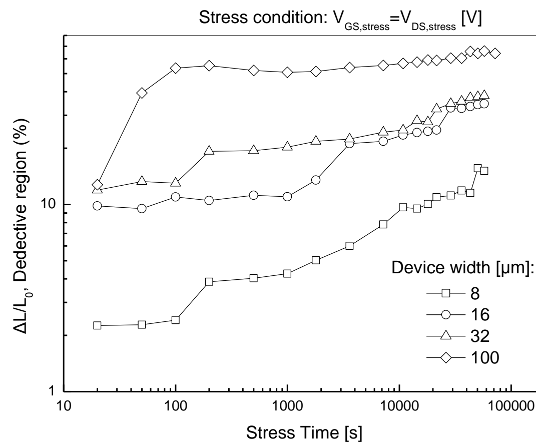


**Fig. 26** Percentage variation of the length of the defective region predicted from the model for devices of various channel widths W = 8, 16, 32 and 100 μm and of a common channel length L = 0.8 μm. Stress condition: $V_{GS,stress} = V_{DS,stress}$

*4.2.6. Double gate TFT degradation mechanisms*

However, attaining high performance is not enough, as one of the major issues associated with polysilicon TFTs is their reliability. The application of bias stress with high drain and gate voltages degrades the performance of TFTs due to hot carrier effects caused mainly by the enhanced field near the drain junction [49]. Even though hot carrier phenomena are widely studied [26, 36, 39], it is not clear yet whether degradation phenomena may also occur at the back interface between the polysilicon film and silicon dioxide, at least for fully depleted TFTs as is the case of fully depleted SOI MOSFETs [50]. The scope of this work [51] is to provide evidences for degradation mechanisms at this back interface of the device, via the aid of fully depleted double-gate (DG) polysilicon TFTs. The investigated TFTs were n-channel double-gate devices. The polysilicon films were formed by excimer laser annealing of amorphous silicon, using the "single-shot" variation of the SLS technique. DC hot carrier stress conditions ($V_{GF,stress}$, $V_{DS,stress}$, $V_{GB,stress}$) were applied for durations up to 27,000 s, the $I_{DS} - V_{GF}$ curves were recorded at the end of each stress cycle with various values of $V_{GB}$ and the device parameters were extracted each time.

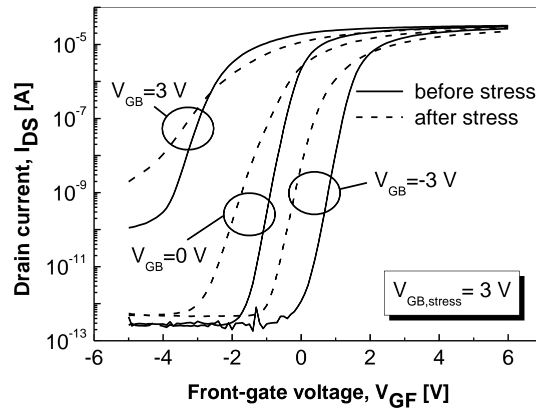


**Fig. 27** Transfer characteristics in linear regime ($V_{DS}$ = 0.1 V) for three back-gate voltages before and after 16,000 s of stress.
Stress condition: $V_{DS,stress}$ = 6 V, $V_{GF,stress}$ = −0.3 V, $V_{GB,stress}$ = 3 V

In the case of continuous hot carrier stress application with inverted back interface ($V_{GB,stress}$ = 3 V), Fig. 27 demonstrates the transfer characteristics before and after aging. In the subthreshold region the drain current increases even for accumulated back interface ($V_{GB}$ = −3 V) and transfer characteristics seem to be shifted in parallel towards negative front gate bias values. In addition, we have to note that the above-threshold current decreases after stress. When the device suffered from a stress condition with depleted back interface ($V_{GB,stress}$ = 0 V), it is observed (Fig. 28) that a minor degradation occurs in the subthreshold region and the main variation comes from the on-current region, where an electron current flows from the front interface. It is also noticed that for $V_{GB}$ = 3 V the current in the off-region, which is mainly controlled by the back-gate voltage, is slightly decreased as compared with the unstressed device. Finally, a stress condition with the back interface in accumulation ($V_{GB,stress}$ = −3 V) was applied. Fig. 29 demonstrates the

drain current variation before and after 16,000 s of stress. It is seen that the on-current is decreased, accompanied by a moderate subthreshold current increase. It has to be added that an important current decrease is observed after stress when the device was back-gate biased at 3 V in the linear regime. Taking into account that the origin of this current comes mainly from the back interface, it is clear that additional hot carrier induced degradation occurred at the back interface.

In the case of $V_{GB,stress} = -3$ V, we mention an elevated dispersion of $V_{th}$ at higher back-gate voltages (i.e., $V_{GB} = 3$ V). This implies that degradation takes place mainly at the back interface of the device. Considering that the back-gate is negatively charged, it is reasonable to believe that hot-holes created by impact ionization at the drain edge region can be easily forwarded at the back interface during stress. Thus, the damaged region is located at the back drain-polysilicon interface. As hot-hole induced damage becomes severe, the threshold voltage increases due to the induced interface state density [26]. At the front interface possibly hot-electrons damage the polysilicon / $SiO_2$ interface and/or the grain boundaries, thus degrading $G_{m,max}$ [50].

In the case of $V_{GB,stress} = 0$ V, $V_{th}$ is decreased by the same amount for all back-gate voltages. The $V_{th}$ decrease appears because of negative voltage shift of entire transfer characteristics. This is possible if we consider that the positive charge in the back oxide increases during aging. Therefore, it is suggested that moderate hot-hole injection occurs into the back-gate oxide with no observable related interface state generation phenomena. Regarding the front interface degradation, since $G_{m,max}$ variation is identical to that for the stress condition $V_{GB,stress} = -3$ V, we propose that the observed degradation arises from hot-electron damage at the polysilicon / $SiO_2$ interface and/or grain boundaries.

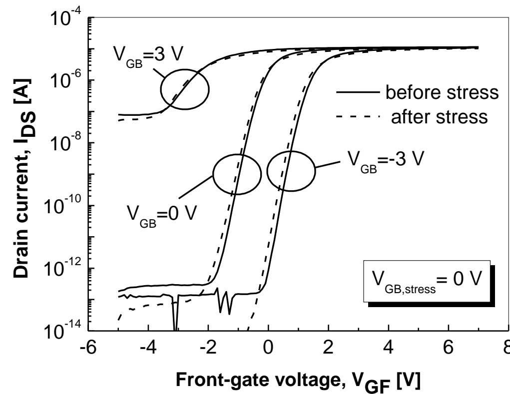


**Fig. 28** Transfer characteristics in linear regime ($V_{DS} = 0.1$ V) for three back-gate voltages before and after 16,000 s of stress.
Stress condition: $V_{DS,stress} = 6$ V, $V_{GF,stress} = -1.8$ V, $V_{GB,stress} = 0$ V

When the device was subjected to a stress condition with $V_{GB,stress} = 3$ V, the threshold voltage decreased for $V_{GB} = -3$ V and increased for $V_{GB} = 3$ V. Moreover, as already mentioned, the $G_{m,max}$ degradation is larger than for previous stress conditions. Since, for $V_{GB,stress} > 0$, the vertical electric field is enhanced, it promotes hot-hole injection in the front interface, while hot-electrons are accelerated towards the back interface. Indeed, under this condition hot-holes and hot-electrons acquire more energy to be directly injected in the

front- and in the back-gate oxide respectively. As a result, hot-hole induced interface state generation is enhanced at the front interface, while electron injection at the back-gate oxide provokes additional negative threshold voltage shift when measured at $V_{GB} = -3$ V.

We proceeded to see whether there are differences in the degradation mechanisms of n-channel and p-channel double gate TFTs of similar dimensions. The bottom gate was biased at −3 V for n-channel devices and at 3 V for p- channel ones, to ensure that all current carriers are pushed towards the top interface. Also, the drain stress biases were scaled with the channel length of the devices to exclude the effect of different horizontal electrical field. The stress condition used was $V_{dstress} = V_{th} + 2$ V for all DG TFTs. As we can see in Fig. 30, for $G_{m,max}$ degradation, we do not see any variation of the associated degradation mechanisms, which concern trap generation within the polysilicon film (particularly at grain boundaries). By reducing the top gate length in n-channel devices; this same mechanism is more intense for larger length. For p-channel devices we see that in short channel devices no significant degradation takes place. In devices having either kind of channel we see that as the channel length increases, device degradation becomes more pronounced, due to the incorporation of more sub-boundary traps within the channel area.

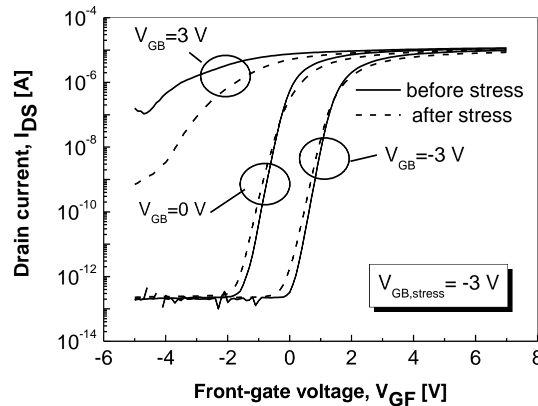


**Fig. 29** Transfer characteristics in linear regime ($V_{DS} = 0.1$ V) for three back-gate voltages before and after 16,000 s of stress.
Stress condition: $V_{DS,stress} = 6$ V, $V_{GF,stress} = 3.5$ V, $V_{GB,stress} = -3$ V

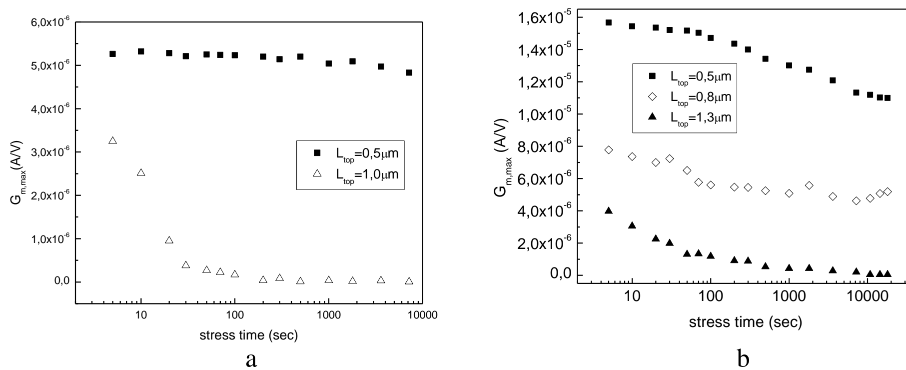


**Fig. 30** $G_{m,max}$ evolution with stress time in (a) p-channel and (b) n-channel double gate devices

However, the threshold voltage $V_{th}$ evolution with stressing time, shown in Fig. 31 for n-channel DG TFTs, indicates that different associated degradation mechanisms, which concern hot carrier injection into generated interface traps and/or the oxide bulk, are present for varying top gate length in these devices. For $L_{top}$ = 0.5 μm we only observe a hot electron injection induced $V_{th}$ increase for larger stress times. For $L_{top}$ = 0.8 μm there is a small initial $V_{th}$ decrease, due to minor hole injection, followed by a pronounced increase for even larger times. For $L_{top}$ = 1.3 μm the initial $V_{th}$ reduction is much more pronounced, again followed by a large increase for long stressing times. It is clear that the initial hole injection mechanism is only present in long channel DG TFTs and becomes more pronounced as the channel gets longer. Electron injection, however, is present in DG TFTs having all top gate lengths and is always dominant for large stressing times. This means that the former, but not the latter, is a channel length dependent degradation mechanism. To further probe the nature of hot carrier injection we also investigated the evolution of subthreshold slope S, which only reflects interface traps, with stress time, and similar trends were observed. This indicates degradation by trap generation mainly at the polysilicon – oxide interface and not by injection in the top gate oxide. The proposed degradation mechanisms are supported by low frequency noise measurements [52].

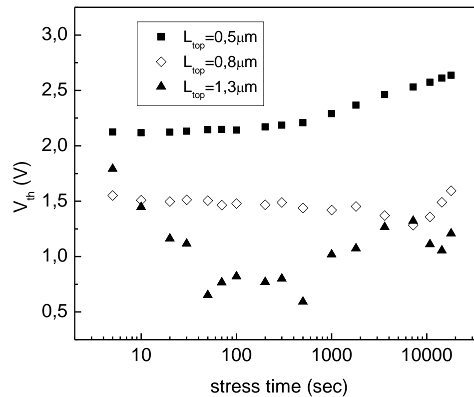


**Fig. 31** Threshold voltage $V_{th}$ evolution with stress time for n-channel double gate TFTs with different $L_{top}$ and $L_{bottom}$ = 4 μm

## 5. CONCLUDING REMARKS AND PROSPECTS FOR SLS ELA TECHNOLOGY

A comprehensive investigation of the performance and degradation characteristics of advanced LTPS TFTs fabricated using several variations of SLS ELA techniques, as resulting from corresponding film microstructures and device geometries, has been presented. The polysilicon film grain structures resulting from these techniques were determined; directional films with elongated grains and various forms of films with engineered grain shapes were obtained. The statistics of the electrical parameter values of TFTs fabricated in such films were extracted. Furthermore, the parameter $V_{g,max} - V_{th}$ was proposed as a new measure of film trap density, in addition to $V_{th}$, $\mu_{fe}$ and S, that mainly probes tail state generation, while S probes midgap states. The effects of the crystalliza-

tion technique, grain boundaries, channel length and channel width on device characteristics were investigated. Moreover, various TFT structures with top, bottom and double gates, for the cases of both n-channel and p-channel devices, were studied and their parameters derived.

The degradation of SLS ELA TFTs fabricated with the aforementioned techniques was investigated for various hot carrier and bias stress conditions. For directional films, the polysilicon film thickness was found to affect which degradation mechanism is dominant. Channel thickness and channel crystal quality are connected, as thicker films have better quality, but were found to exert independent effects on TFT degradation; hot-carrier injection was the primary degradation mechanism for thinner TFTs (due to more carrier trapping, related to worse crystal quality) and for thicker ones (due to partial depletion, related to thickness), while maximum degradation, associated with new defect creation, was only dominant for intermediate thickness (50 nm). Degradation was less pronounced in the non-preferred Y direction, due to the harder sub-boundaries obstructing the stress current. The main degradation mechanism for the X direction was interface state generation, while for the Y direction the gate oxide charge injection. We also observed channel shortening effect only in the X direction. Finally, an optimum channel length was found, defined both by the process related sub-boundary characteristics and by electrical effects.

For various kinds of SLS ELA films, the effects of channel type, width and orientation with respect to engineered grains, as well as the short channel effects were investigated. A simple and practical degradation model was developed, taking into account the formation of two regions, a defective and a non-defective one, in the stressed device. For single-shot directional SLS ELA polysilicon TFTs, larger channel widths resulted in devices exhibiting HCS degradation mainly due to more energetic hot electrons and thus enhanced electron injection in the gate oxide, while for smaller widths hot-holes are mainly responsible for the degradation. The quality characteristics of the width depended degradation were evaluated by the model and the defective region length was found to depend on channel width, with a different dependence for each stress regime studied. It was found that the channel width affects the intensity and not the mechanism of degradation.

Furthermore, the degradation mechanisms pertaining to double gate TFTs were investigated and described. Various degradation mechanisms that depend on the back gate voltage were identified and evaluated. Double gate TFTs for various channel lengths were characterized; degradation was found to be more pronounced for longer channel devices, due to the existence of more grain boundaries and sub-boundaries, resulting in more trap generation. We observed two $V_{th}$ degradation mechanisms, hole injection only in large channel DG TFTs and electron injection in all devices for longer times; considering additional S degradation data, these mechanisms were ascribed to interface trap generation.

As we can see from the previous analysis, the several variations of SLS ELA technology can yield very high-performance and highly reliable TFTs, comparable to SOI transistors. This fact, with the added advantage of being able to integrate such devices on various low temperature substrate materials (e.g. polymer, paper, foil etc), could open up new prospects for high performance macroelectronic applications. Further integration with other low-temperature devices (e.g. OLEDs) could allow stretchable or foldable, high performance commercial electronics, since the excellent SLS ELA TFT characteristics allow for advanced CMOS circuit design. Also, high performance TFTs could allow for their utilization as versatile (due to the freedom to choose a substrate of choice other

than Si wafers) physical, chemical or biological sensors. Their optimum mobility can yield very sensitive, and highly conducive to integration, sensing devices, possibly allowing for "smarter" micro Total Analysis Systems (μTAS) with the integration of microfluidic networks.

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