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# MULTIPLE PURPOSE SPIN TRANSFER TORQUE OPERATED DEVICES

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**Abstract**. *We summarize our recent work on a non-volatile logic building block required for energy-efficient information processing systems. A sequential logic device, in particular, an alternative non-volatile magnetic flip-flop has been introduced. Its properties are investigated and its extension to a very dense shift register is demonstrated. We show that the flip-flop structure inherently exhibits oscillations and discuss its spin torque nano-oscillator properties.*

**Key words**: *spin transfer torque, non-volatile logic, flip-flop, latch, shift register, nano-oscillator*

## 1. INTRODUCTION

Due to the rising efforts to scale CMOS devices down with every technology node, according to the ITRS [1], new technological processes incorporating global and local strain, new materials for high-k/metal gates, and new fin-FET and three-dimensional tri-gate device structures must be introduced. At the same time power consumption and interconnect delay start to become an important performance bottleneck [2]. One possible way to reduce the power consumption of CMOS circuits is to shutdown latent circuit parts completely and to power them up only when they are needed. This transition from normally "ON" to normally "OFF" circuits requires the successive reevaluation of all computational building blocks. The use of non-volatile elements which do not need power to keep their state is paramount for the success of this new type of information processing. At this point the exploitation of spin as degree of freedom comes in handy, due to its non-volatility, high endurance, and fast operation [3]. Furthermore, it allows not only to store information efficiently, but also to introduce new approaches to how the actual information is processed and the information transport is handled [4], [5]. Thus, it also allows to look for alternatives to the von Neumann architecture, where successively information is moved between the memory unit and the processing unit through a - nowadays performance limiting - common bus.

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The most obvious potential application of non-volatile spintronic devices as CMOS alternative is dynamic and static random access memory. The discovery of the giant magneto resistance (GMR) [6], [7] and the tunnel magneto resistance (TMR) [8] effects further boosted interest in magnetic devices, which results in improving their performance and bringing them to commercial applications [9], [10]. At its earlier stage this research led to the development of magnetic memory arrays [9], [11] for random access memory applications: MRAM. Initially, their logic states had to be written by a magnetic field, requiring an extra wire for field generation. Unfortunately, this caused high writing energies and unfavorable scaling behavior and thus was prohibitive for (very) large scale integration (VLSI). This problem was resolved by first theoretically predicting and later experimentally justifying the spin transfer torque effect [12], [13]. The spin transfer torque (STT) effect allows a purely electric control of the magnetization orientation and thus leaves the writing wire generating the magnetic field in MRAM superfluous. However, the current value needed to invert the magnetization of the free layer in magnetic tunnel junction (MTJ) is still rather high, and its reduction is the main goal of research to make this technology competitive with CMOS. Utilization of MTJs with perpendicular magnetic anisotropy allows reducing the required writing power to a level, where it can compete with CMOS SRAM cache [14], [15], [16], [17]. Several products based on spin transfer torque magnetic random access memory (STT-MRAM) technology have been recently introduced [18], [19], [20], [21].

However, besides the apparent MTJ applications for memory cells, new spintronic devices open up additional opportunities for replacing CMOS based counterparts [3]. Below we introduce a non-volatile magnetic flip-flop as an information processing unit.

## 2. Non-Volatile Magnetic Flip-Flop

As already mentioned, the ever increasing demand in fast and cheap memory as well as in electronics in general has driven the scaling efforts in CMOS since its very beginnings. Today, pushing the limits of integration density is still a major concern, but power efficient computing gains more and more momentum. In addition to memory and combinatorial logic mostly employed in modern integrated circuits, sequential logic attracts close attention. Sequential logic can be based on memory elements for information processing. Its present output states not only depend on its present inputs, but also on its input history [22]. Sequential logic devices are fundamental building blocks of digital electronics, and flip-flops as well as latches belong to this group of logic. The transition from normally "On" to normally "Off" logic requires a redesign of these devices as well.

Even though already several circuit designs have been proposed to meet this goal, e.g., Zhao et al. [23], these circuits are commonly CMOS-MTJ hybrids. The non-volatility is introduced by the MTJs, however, the MTJs act merely as ancillary devices by only holding the information without any further functionality. The actual logic operations are carried out in the CMOS elements. The introduction of non-volatility through MTJs adds complexity because of the need for converting the information between resistance states of the MTJs and voltage or current signals required for CMOS operation every time data is written, read, or transferred.

Therefore, we propose a novel non-volatile magnetic flip-flop which shifts the actual logic operation and thus the information processing from the electric signal CMOS domain to the magnetic domain [24]. This allows creating denser and simpler layouts as well as harvesting the beneficial features related to spintronics.

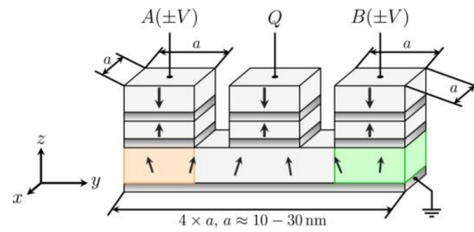


**Fig. 1** Proposed non-volatile magnetic flip-flop

### 2.1. Structure and working principle

The non-volatile magnetic flip-flop consists of three fixed anti-ferromagnetically coupled polarizer stacks (see Fig. 1). Two polarizer stacks are for input (A, B) and one polarizer stack is for readout (Q). They exhibit a fixed perpendicular magnetization orientation (parallel to the z-axis) and due to their anti-ferromagnetic configuration negligible stray fields are assumed. The polarizer stacks are positioned on top of tunnel barriers (e.g. Cu, $Al_2O_3$, and MgO) and share a common free layer. The common free layer exhibits a perpendicular anisotropy with a constant uni-axial anisotropy $K_1$ (parallel to the z-axis). It is further assumed that the ratio of the common free layer is 4 to 1 with the size of the short side of the layer ranging from 10 nm to 30 nm. The long side of the free layer is along the y-axis, while the short side lies parallel to the x-axis.

Furthermore, a positive electric current is defined as flowing from the contacts (A, B, Q) through the free layer (negative z-direction), while at the same time electrons flow in the opposite direction (positive z-direction).The logic information is stored via the magnetic orientation of the free layer, and the polarity of the input pulses is mapped to logic "0" and "1", respectively.

A current pulse applied to one of the input stacks (A or B) exerts a spin transfer torque on the magnetization in the corresponding free layer region of the input stack and generates a precessional magnetization motion. This precessional motion couples through the magnetic exchange to the rest of the free layer and creates a spin wave which travels through the common free layer heading to its opposite end, where it is reflected and moves back, gets reflected, and pushed again and so on [25]. During this kind of oscillating spin wave motion, the localized magnetic moments in the common free layer are excited and their precessional motions build up, until the magnetization eventually passes the energy barrier between the two stable states and relaxes into the other stable state fast. If now, instead of one, two synchronous current pulses are applied to the input stacks A and B, two moving spin waves are generated. Depending on their polarity they either try to enforce the switching of the free layer magnetization or hold it in its current position.

There are four possible input combinations. In the case of two positive currents both generated torques align the magnetization parallel to the z-axis. Therefore, the magnetization orientation stays unchanged. If both input currents are negative, both generated

torques try to flip the magnetization orientation. In this case both spin waves add up leading to a faster switching compared to a single input current. Finally, in the case of opposing input current polarities one torque always tries to hold the current magnetization state, while the other strives to flip it. Since these two contributions compensate each other, the magnetization direction of the free layer remains the same.

Thus, two sufficiently high and long pulses with identical polarity either write logic "0" or "1" into the common free layer, while two pulses with opposing polarities cancel each other and the initial magnetization state is held representing a sequential logic function needed for flip-flop logic. If one of the inputs is inverted, the resulting logic sets or resets the held state, when the input signals are opposing, and holds its state for identical input polarities. This corresponds to RS flip-flop logic, but without forbidden input combinations as compare to its transistor counterpart [22].

### 2.2. Device characteristics

In order to test our proposed device a series of micromagnetic simulations was carried out [26], [27]. Three different free layer sizes with length to width ratio of four to one were studied. It was further assumed that the common free layer featured layer widths of 10nm, 20nm, and 30nm, a layer thickness of 3nm, a perpendicular uni-axial anisotropy $K_1=10^5$ J/m$^3$ along the z-axis, and that the spin barrier connecting the polarizer stacks to the free layer is made out of copper (cf. Fig. 1). The saturation magnetization of the common free layer was considered as $M_S=4\times10^5$A/m, an exchange constant of $A_{ex}=2\times10^{-11}$J/m, and a spin current polarization P of 0.3. As mentioned in Section 2.1, the polarizer stacks consist of anti-ferromagnetically coupled layers. Therefore, stray fields are neglected.

The magnetization dynamics is described by the Landau-Lifshitz-Gilbert equation [28], [29]:

$$\frac{d\vec{m}}{dt} = \gamma\left( -\vec{m}\times\vec{H}_{eff} + \alpha\left(\vec{m}\times\frac{d\vec{m}}{dt}\right) + \vec{T}\right), \tag{1}$$

where $\vec{m}$ denotes the reduced magnetization, $\gamma=2.211\times10^5$m/As the Gilbert gyromagnetic ratio, $\alpha = 0.01$ the dimensionless damping constant, $\vec{H}_{eff}$ the effective field in A/m. The last term in (1) describes the spin transfer torque $\vec{T}$ with the following spin transfer torque model [30]:

$$\vec{T} = \frac{\hbar}{\mu_0 e}\frac{J}{l M_S}\frac{P\Lambda^2}{(\Lambda^2+1)+(\Lambda^2-1)\vec{m}\cdot\vec{p}}(\vec{m}\times\vec{p}\times\vec{m} - \varepsilon'\vec{m}\times\vec{p}) \cdot \tag{2}$$

$\hbar$ denotes the Planck constant, $\mu_0$ the permittivity of vacuum, $e$ the electron charge, $J$ the applied current density, $l$ the free layer thickness, $M_S$ the magnetization saturation, $P$ the polarization, $\vec{p}$ the unit polarization direction of the polarized current, and $\Lambda=2$ a fitting parameter handling non-idealities. Furthermore, $\vec{H}_{eff}$ is calculated from the functional derivative of the free energy density functional containing uni-axial anisotropy, exchange, and demagnetization contributions [31].

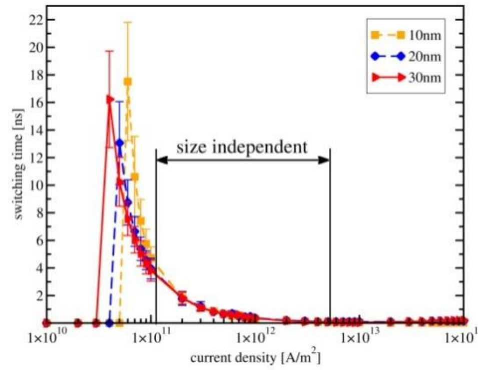


**Fig. 2** Switching times for identical input pulses as a function of applied current density

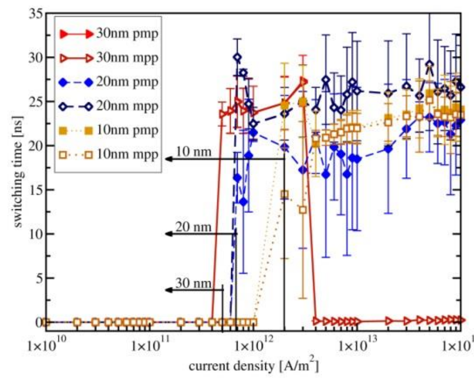


**Fig. 3** Switching times for opposing input pulses as a function of applied current density. m denotes a negative polarity current pulse, while p denotes a positive polarity current pulse. For instance *pmp* (A, B, free layer) means a positive current pulse applied at contact A, a negative current pulse applied at B, and a magnetization orientation of the free layer along z-axis

The data points in Fig. 2 and Fig. 3 are averaged over 100 samples. The error bars depict an error range of $\pm 3\sigma$. Fig. 2 shows the switching times for the set and reset operation as a function of applied current densities and different layer sizes. The corresponding switching times are defined as the time it takes from the onset of the current pulse until 80% of the final magnetization state is reached. One can see that at low current densities it takes relatively long to build up the required precessional motion for flipping the layer magnetization, while with increasing current densities the switching times decreases fast. The difference in the threshold current densities for different geometries can be explained as follows. Reducing the layer width reduces the demagnetization factor along z but at the same time the demagnetization factors along x and y start to increase [32]. This leads to a smaller depolarization field along z and a bigger net barrier parallel to the z-axis, since the depolarization field opposes the anisotropy field. Therefore, the smaller the layer width the higher is the switching barrier and the required current to pass the barrier. For a pulse length of 20ns switching starts at $4\times10^{10}$A/m$^2$ (16±3.5ns), $5\times10^{10}$A/m$^2$

(13±3ns), and $6\times10^{10}$A/m$^2$ (17.5±4.3ns) for 30nm, 20nm, and 10nm width, respectively. It is worth to mention that, the switching speed becomes almost size independent around ≈$10^{11}$A/m$^2$ until ≈$5\times10^{12}$A/m$^2$ and the found switching times are in the order of ≈20ps to ≈100ps.

In contrast to the set and reset operation, the hold operation must not lead to a change in the magnetization state. This is the case at opposing input pulses (see Fig. 3). For a reliable flip-flop operation the magnetization $\vec{m}$ must relax back to its initial orientation, when the currents are turned off. Starting with an initial magnetization state along the positive z-axis (as shown in Fig. 1), the total average magnetization projection should not become negative during its precessional motion. If the magnetization overcomes the state separating energy barrier and its projection on the z-axis becomes negative ($m_z < 0$), the final magnetization state starts to depend on the pulse length. In other words, this is the point, when the held information is lost.

The devices behave as required for current densities below $2\times10^{12}$A/m$^2$ for 10nm width, $7\times10^{11}$A/m$^2$ for 20nm width, and $5\times10^{11}$A/m$^2$ for 30nm width (cf. Fig. 3). Close to the respective current densities the spin wave generated at A (B) is not sufficiently damped anymore and oscillatory motions start to build up. In fact, above the shown limits the oscillations can become so strong that they cross the xy-plane and the initial magnetization orientation is lost. Due to the geometrical confinement the oscillation frequencies of the excited spin waves as well as the onset current densities for their excitation depend on for the shared free layer sizes.

Already at this point the proposed non-volatile magnetic flip-flop is very attractive. In addition, it requires less space than its CMOS counterparts, e.g., eight or twelve transistors for a classical simple or clocked RS flip-flop, correspondingly [22], and it is also more space efficient than hybrid MTJ/CMOS circuits, for example, the flip-flop proposed in [23], which requires seven transistors and two magnetic tunnel junction memory elements.

Instead the non-volatile magnetic flip-flop needs only three magnetic stacks (spin valve and/or MTJ) sharing a common free layer. Even more, there are no forbidden input combinations ($R = S = 1 \rightarrow Q = \bar{Q} = 0$) making the circuit and logic design easier. Due to its back end of line compatibility and stack friendly topology (see Fig. 4), it is also attractive for large scale integration.

### 2.3. Shift-register

In [33] we proposed an application of the flip-flop for a non-volatile shift register. The shift register features an extremely dense layout and allows further reduction of the required space (cf. Fig. 4).

The novel shift register topology takes advantage of the peculiarities of the non-volatile flip-flop. Arranging two rows of flip-flops in two different levels along a line (as shown in Fig. 3) or in a cross-like structure [33] and applying two time shifted clock signals ($Clk_1$ and $Clk_2$, see Fig. 5 and Fig. 6), the information contained in one flip-flop can be successively passed to the next subsequent flip-flop via the STT effect.

The shift register works as follows. Each flip-flop is alternately operated in a writing and a reading mode. In the writing mode the inputs $A_i$ and $B_i$ are active, while $Q_i$ is inactive. In this mode one input is fed with the information/signal while the other is fed by one of the two clock signals (depending on its level, cf. Fig. 5). In the reading mode $A_i$

and $B_i$ are inactive and $Q_i$ is active. A save decoupling between the two operation modes is achieved by a time shift between the two clock signals (see Fig. 6).

In order to avoid the unintentional flipping of the common free layer (also known as read disturbance), the pulse time mismatch between the reading and writing mode is used. While in reading mode only the part of the common free layer under the $Q_i$ region experiences a spin torque, in writing mode two regions $A_i$ and $B_i$ exert a spin torque on the common free layer. Therefore, it takes about twice as long to change the magnetization orientation in reading mode than in writing mode provided the currents are the same. Let us illustrate the working principal with an example (see Fig. 4, Fig. 5, and Fig. 6). Applying an input pulse to $A_1$ and a first clock signal $Clk_1$ to $B_1$ to the first flip-flop (Fig. 4, left) will set or reset the flip-flop, if both pulses exhibit the same polarity. When the input signal and the clock signal $Clk_1$ exhibit the same torque on the shared free layer, information is written into the first free layer and can be accessed via $Q_1$. At the next step clock signal $Clk_1$ turns inactive and $Clk_2$ becomes active (cf. Fig. 6). This time the first flip-flop is in reading mode and a current passes through the first free layer and the spin barrier separating the two neighboring free layers before it enters to the second free layer and exerts a spin torque on the second free layer. At the same time the clock signal $Clk_2$ creates spin torque in the $B_2$ region and the interaction between the two spin torque sources either aids or suppresses the switching of its magnetization state. Afterwards the clock signal $Clk_2$ is switched off again and the clock signal $Clk_1$ is turned on. Hence, the second flip-flop is now in reading mode and information is passed via the STT effect to the third free layer and so on. It is necessary to mention that the voltage or current signals passing the information at $Q_i$ must be synchronized with respect to the corresponding clock signals and that due to the additional degree of freedom introduced by the variable shared free layer magnetization, $Q_i$ must be fed with one type of polarity only. This is necessary to compensate the changing free layer magnetization in region $Q_i$. The clock signals $Clk_1$ and $Clk_2$ require a positive and negative pulse within their signal period to guarantee that the information stored in one shared free layer will be successfully passed into the next subsequent flip-flop, since only by two identical input pulses the flip-flop is written.

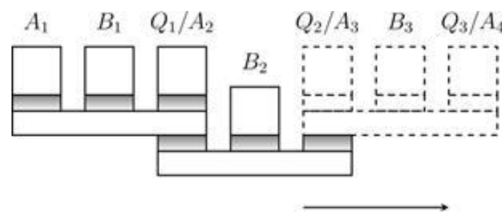


**Fig. 4** Proposed non-volatile magnetic shift register

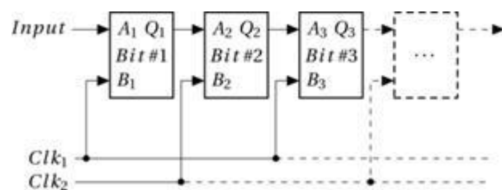


**Fig. 5** Circuit diagram of non-volatile magnetic shift register

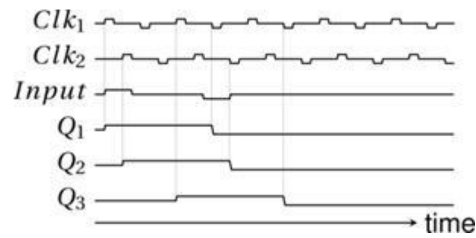


**Fig. 6** Signal timing example for the non-volatile magnetic shift register showing the successive propagation of the input signal through register

### 2.4. Intrinsic oscillator

Despite its use as a sequential logic building block the flip-flop structure also features large and stable oscillations (see Fig. 3 and Fig. 7). This is bad for logic applications, but quite appealing for exploitation as a nano-scale oscillator. Oscillators constitute a very basic building block and are ubiquitous in modern electronics. They are needed in measurement, navigation, communication systems, and more. Their periodic output signals are used manifold, for example, for clocking digital circuits, generating electromagnetic waves, in high speed digital systems, and many more. Spin torque nano-scale oscillators are so attractive because of their cost effective on-chip integration as microwave oscillators, their nano-scale size, frequency tunability, broad temperature operation range, and CMOS technology compatibility [34], [35], [36], [37], [38]. Even though substantial progress has been achieved and they can now operate without an external magnetic field, their still rather low output power limits their practical implementation [39], [40].

As discussed in Section 2.2, we observe oscillations in the common free layer, if current densities with opposing polarities above the respective thresholds are applied (shown in Fig. 3) [33], [41]. The excited precessional motions form large and stable orbits and do not require an external magnetic field (see Fig. 7).

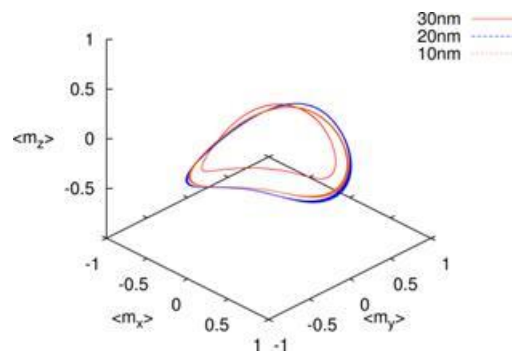


**Fig. 7** Plot of the averaged and normalized magnetization of the common free layer for 10nm, 20nm, and 30nm, respectively

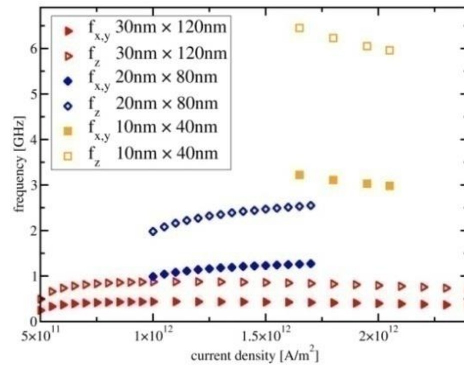


**Fig. 8** Frequency as a function of applied current density and free layer size

The occurring precessional motions are a superposition of two movements - an in-plane precession ($f_{x,z}$) and an out-of-plane oscillation ($f_z$). Plotting the found oscillation frequencies as a function of applied current density and free layer size shows that for a fixed current density the frequency $f_z$ for the out-of-plane component oscillations (filled symbols) is two times the corresponding in-plane precession $f_{x,y}$ frequency (open symbols). It also can be observed that for different shared free layer sizes the precessional frequencies change (see Fig. 8). For the 30nm×120nm structure the stable precessional motion starts at ≈250 MHz (≈$5\times10^{11}$A/m$^2$) and increases up to ≈450 MHz ($1\times10^{12}$A/m$^2$), while for 20nm×80nm the precessions start at ≈1 GHz ($1.\times10^{12}$A/m$^2$) and increases to ≈ 1.17 GHz ($1.25\times10^{12}$A/m$^2$). For the 10nm×40nm structure they range from ≈3.22 GHz ($1.6\times10^{12}$A/m$^2$) to ≈ 3 GHz ($2.05\times10^{12}$A/m$^2$).

Further analysis shows that in the case of a single pulse at one input polarizer the magnetization of the free layer is inverted, even though the generated spin torque acts only on the free layer below the corresponding polarizer stack. Therefore, in this setup two input pulses are required for the generation of oscillation. This hints already to the explanation how the oscillations are excited. For example, if a positive current pulse is applied through region A (shown in Fig. 1), the generated polarized current will exert a spin torque on the local magnetic momenta and excite local precessional motions, which try to flip the free layer magnetization. Through the exchange coupling these precessional motions start to move out of the region where they are generated and travel through the whole free layer (also known as spin wave). When the spin wave reaches the opposite end of the free layer (B), it experiences a second torque which tries to preserve the magnetization orientation of the free layer (negative current). The wave gets reflected, heads back to region A where it is pushed out again, and so on. The result is a stable precessional motion in the whole free layer. This explanation is consistent with the time and position resolved magnetization simulations we conducted and also explains the dependence of the frequency on the free layer size [38]. While other groups reported a localization of the oscillations below the spin injection site, in our device the full layer contributes to the precessions [36], [37], and [38]. We think this difference stems from the rather strong stray field in the setups used in [36], [37], and [38], while in our case the stray field is negligible.

However, in order to extract power from the oscillator the projection of the precessional motion on the pinned layer magnetization orientation should be as big as possible.

Unfortunately, the perpendicular polarizers (see Fig. 1) lead to an extraction of the much weaker vertical oscillations $f_z$ (see Fig. 7). A possible way to circumvent this obstacle is to change the orientation of the output polarizer $Q$ to an in-plane configuration and extract the signal from there. Thus, the much bigger $m_{x,y}(t)$ component can be used. But this also comes at a price; since the power extracted from $Q$ is proportional to the power put through $Q$, it must be sufficiently small to not disturb the oscillations.

Therefore, one might instead of changing $Q$ to an in-plane orientation, modify $A$ and $B$ to in-plane configurations [39]. This case was tested in [41], where it was shown that the free layer magnetization also preforms large in-plane precessions. The observed stable oscillations exist even when the current is driven through a single stack. The current through the second stack allows tuning the frequency. If the current through the second stack exhibits the opposite polarity, the frequency of the oscillations is almost doubled. Because of the in-plane orientations of the polarizer stacks, the large $m_{x,y}(t)$ component is extracted and the available microwave power is increased. Because the whole free layer exhibits the oscillations when the excitation sources are at its opposite ends, wireless power extraction and further distribution is an interesting option for this structure.

## 3. Outlook and Conclusion

Even though great progress has been made over the last years, there are still challenges to be resolved to bring spintronics into mainstream electronics. One reason is the maturity and excellence of CMOS technology itself. While the switching power of STT based memory has become comparable with that of CMOS based SRAM and DRAM [10], [14], [15], [16], and [17] its integration density is currently not as good as in state of the art CMOS solutions. Spintronics for logic applications is under extensive development. One of the show stoppers is the rather high energy required for switching: switches based on the STT effect require still about 100 times more switching power than a CMOS transistor [3]. Thus, the real challenge to bring the spin-driven devices close to commercial applications is to reduce the required switching power for memory and logic. For STT based nano-oscillators an increase of the output power is a pressing issue. A promising path to reach this goal is to migrate from current controlled switching to voltage controlled switching. There are many promising results related to the voltage control of magnetic properties. For instance, Wang et al. [42] have shown electric-field-assisted reversible switching in CoFeB/MgO/CoFeB magnetic tunnel junctions with interfacial perpendicular magnetic anisotropy, where the coercivity, the magnetic configuration and the tunneling magnetoresistance can be manipulated by voltage pulses associated with much smaller current densities ($\approx 1.2\times10^6$A/m$^2$). Despite the critical switching power reduction also other essential features like fast switching in the below nanosecond regime [43] and voltage control of the exchange bias at room temperature have been demonstrated [44]. It also has been shown by Nozaki et al. [45] that electric-field-induced ferromagnetic resonance excitation by means of voltage control over the magnetic anisotropy in a few monolayers of FeCo at room temperature is feasible. So we conclude that there is still plenty of space left to explore and to further develop spintronics and its application in large scale applications.

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