FACTA UNIVERSITATIS
Series: **Electronics and Energetics** Vol. 26, N° 3, December 2013, pp. 197 - 213
DOI: 10.2298/FUEE1303197C

REVIEW ON DOUBLE-GATE MOSFETS AND FINFETS MODELING

A. Cerdeira[1], M. Estrada[1], J. Alvarado[2], I. Garduño[2], E. Contreras[1], J. Tinoco[3], B. Iñiguez[4], V. Kilchytska[5], D. Flandre[5]

[1]Solid-State Electronics Section, CINVESTAV, Av. IPN 2508, Mexico DF, C.P. 07360 Mexico
[2]Centro de Investigación en Semiconductores, BUAP, Edif. 137 Av. Sn. Claudio esq. 14 Sur s/n, Ciudad Universitaria, C.P. 72570 Puebla Pue., Mexico
[3]Centro de Investigación en Micro y Nanotecnología, Universidad Veracruzana, CP 94294, Veracruz, México
[4]Universitat Rovira I Virgili, Av. Paisos Catalans 26, 43007 Tarragona, Spain
[5]ICTEAM Institute, Universitet catholique de Louvain (UCL), Place du Levant 3, B-1348, Louvain-la-Neuve, Belgium

Abstract. *The development of compact models for double-gate (DG) MOSFETs and FinFETs necessary in circuit simulators is an important research field, which allows the efficient practical characterization of these devices, as well as their application in analog circuit design. In this paper we review and assess different approaches for developing core and complete compact models for DG MOSFETs and FinFETs*.

Key words: *DG MOSFET modeling, FinFET modeling, compact modeling*

1. INTRODUCTION

The Double-Gate (DG) MOSFET was proposed in 1987 [1] and studied in more detail later on [2]. Among the advantages of this fully depleted transistor are: the increase of the amount of current provided by the device, for the same channel length, as well as a better electrostatic control of the silicon layer leading to the reduction of the short-channel effects (SCE). Since then, a significant amount of work has been done in order to achieve its technological implementation/maturity, as well as to improve a modeling of its behavior. The best transistor structure was obtained using a vertical silicon layer (fin) with two lateral gates. The introduction of a top gate results in a triple gate transistor, (trigate), which is a real 3D transistor structure with two lateral channels. The lateral transistors have reduced mobility due to the crystal orientation, compared with the top channel transistor, with standard mobility. This kind of transistor structure received the name of FinFET.

Received November 8, 2013
Corresponding author: A. Cerdeira
Solid-State Electronics Section, CINVESTAV, Av. IPN 2508, Mexico DF, C.P. 07360 Mexico
(e-mail: cerdeira@cinvestav.mx)

The transistor channel width of one FinFET is defined by the fin width W_{FIN} and fin height H_{FIN}; see Fig 1, giving a transistor width W_1 equal to $2H_{FIN}+W_{FIN}$. The necessary current level is obtained by fabricating multiple fins n_{FIN} in parallel, obtaining a final total transistor width W equal to n_{FIN} xW_1. In many cases, especially when H_{FIN} is at least twice W_{FIN}, the FinFET can be considered a DG transistor where the channel width can be considered $H_{FIN}+W_{FIN}/2$, and for this reason, the development of FinFET models is related to the development of DG models. Besides, in the case when the applied gate voltage and the gate dielectric layer are identical for both gates, we have a symmetrical DG MOSFET. DG MOSFETs have other advantages over single-gate transistors, as a practically ideal subthreshold swing close to 60 mV/dec for long channel devices, which increases up to 70 mV/dec for L= 40 nm and a better I_{on}/I_{off} ratio. These transistors can be fabricated using SOI wafers (SOI FinFETs) or standard bulk wafers (Bulk FinFETs). The fabrication process of these bulk FinFETs is reported to be compatible with standard CMOS technology [3].

Perspectives of DG MOSFET for analog applications have been extensively studied, in [3]-[6]. These applications require an accurate compact model, continuous in all operation regimes, as well as with continuous derivatives in order to describe well the non-linear transistor distortion, which is the main problem for analytical DG MOSFETs modeling.

In contrast with standard MOSFETs, DG transistors with fully depleted silicon layer have a distribution of the electrical potential inside the layer, where the potential at the center being different from zero. The potential at the surface and at the center are coupled. In this case, the surface electric field depends on the difference of potentials at the surface and at the center of the film and the surface potential equation, as function of gate and drain voltages, is transcendental and can be exactly solved only numerically.

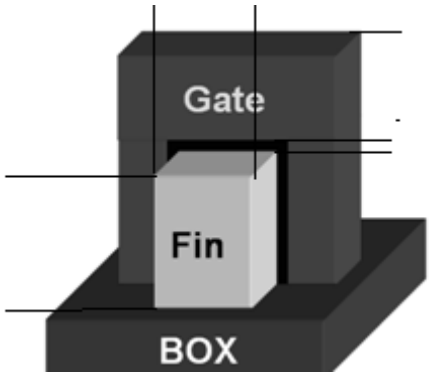

Fig. 1 Structure of a FinFET. H_{FIN}- fin height; W_{FIN}- fin width; t_{OX}- equivalent oxide thickness; t_{gate}- gate thickness

One approach for DG MOSFETs study and modeling is the detailed analysis of the behavior of some of their parameters as the threshold voltage [7]-[9], or the characteristics of some operating region, as the subthreshold region [10], [11], for which 2D and 3D simulations are an important tool.

The physical behavior of DG MOSFETs can be represented as a function of the device structure, technological parameters and applied external voltages. These expressions

are difficult to introduce in compact device models, however, simpler quasi empirical expressions can be derived from them.

Another approach is the development of compact models, which can be introduced in circuit simulators allowing the practical characterization, as well as both digital and analog circuit design.

The requirements for such DG MOSFET compact models include, among others: i) to be physically based and continuous from subthreshold operation region to strong inversion region; ii) to provide continuity of currents and their derivatives as function of applied voltages in all operating regions; iii) to be symmetrical around V_D= 0V and fully analytical; iv) to consider variable mobility and silicon layer doping concentration from undoped to highly doped; v) to compute the total mobile charge inside the silicon layer describing the full inversion condition; vi) to include the dependence on temperature and on structures dimensions, as well as the short channel effects on threshold voltage, on subthreshold swing and on channel length modulation. Finally they should be accurate and computationally efficient.

The Short-Channel effects (SCE) are introduced in the core models as complements based on physical and empirical expressions. Quantum Mechanical effect (QM) is necessary to be introduced in the model when the silicon layer is thinner than 10 nm.

In the following sections we assess different approaches that have been reported to develop core and complete models for DG MOSFETs and FinFETs.

2. Modeling Highly-Doped DG MOSFETs

Among many efforts to develop a core model for long channel DG MOSFETs, in the first years, when the polysilicon gates were used and a highly-doped silicon layer was necessary, models were developed for that condition. In this case some simplifications can be done that allowed the development of approximate analytical models, like [12]-[14].

3. Modeling undoped DG MOSFETs

The simplest case is when the silicon layer is considered to have intrinsic doping concentration, which at that time was named the undoped case. A review of models for undoped DG MOSFETs was presented in [15]. In all cases, 1D Poisson equation was solved for a core model, considering long channel and constant mobility. Short-channel effects (SCE) were introduced later as complements to the 1D I-V equations.

Among the first papers on DG MOSFET models was also a threshold voltage type compact model [16] for undoped silicon layer. Starting from 2000, a continuous flow of model proposals has been published. We will briefly describe some of them, starting with model approaches for undoped DG MOSFETs and FinFETs.

A) Taur and coworkers work

From 2000 to 2006, Taur and coworkers presented the solution of the DG MOSFET equations considering the silicon layer to have intrinsic doping concentration, n_i, that is, the undoped case [17], [18]. The Poisson equation was solved for the case of intrinsic doping concentration as follows, i.e. neglecting fixed charges:

$$\frac{d^2\varphi}{dx^2} = \frac{q\,n_i}{\varepsilon_s} e^{\frac{\varphi - V}{\varphi_T}}, \tag{1}$$

where φ changes across the thickness of the film and V changes along the channel.

After two integrations, the surface potential φ_S along the channel is obtained as function of a constant intermediate calculation parameter β:

$$\varphi_S(x) = V - 2\varphi_T \ln\left[\frac{t_S}{2\beta L_{Di}} \cos\left(\frac{2\beta}{t_S} x\right)\right], \tag{2}$$

where t_s is the silicon layer thickness, L_{Di} is the intrinsic Debye length and φ_T is the thermal voltage kT/q.

The boundary condition at the surface was calculated as:

$$\frac{V_{GS} - \Delta\phi - V}{2\varphi_T} = \ln\beta - \ln(\cos\beta) + 2r\beta\tan\beta\ , \tag{3}$$

where $r=C_S/C_{ox}$, C_S is the silicon layer capacitance, C_{ox} is the gate dielectric capacitance and the mobility is considered to be constant. The drain current was calculated as:

$$I_{ds}(\beta_s, \beta_d) = \mu \frac{W}{L} 8C_S(\varphi_T)^2 \cdot \left[\beta\tan\beta - \frac{\beta^2}{2} + r\beta^2\tan^2\beta\right]_{\beta_d}^{\beta_s} \tag{4}$$

Total charge and capacitance are functions of β too. The procedure for the calculation of β at source and drain (β_s and β_d) is the solution of the following system of two equations:

$$\frac{V_{gs} - \Delta\phi}{2\varphi_T} - \ln\left[\frac{2L_{Di}}{t_S}\right] == \ln\beta_s - \ln(\cos\beta_s) + 2r\beta_s\tan\beta_s \tag{5}$$

and

$$\frac{V_{gs} - \Delta\phi - V_{ds}}{2\varphi_T} - \ln\left[\frac{2L_{Di}}{t_S}\right] == \ln\beta_d - \ln(\cos\beta_d) + 2r\beta_d\tan\beta_d\,. \tag{6}$$

These implicit equations can be solved graphically [17], or numerically by first or second-order Newton-Raphson method [18], although authors considered this solution as analytical.

In 2007, in [19], [20], this group adopted the algorithm proposed_from PSP for the *approximate solution* of surface potential [21], again for undoped transistors. This procedure is complex and their steps are the followings:

1. Compose a continuous starting function, f(β), as the initial approximation to determine β. The implicit equations are simplified at strong inversion and subthreshold and obtained results are sewed by a smoothing function. A well defined initial function is very important for the final solution

2. Modify the starting function with high order correction. If the implicit equation is equal to $f(\beta)=0$ and their derivatives are:

$$f_n = \left.\frac{\partial^n f}{\partial \beta^n}\right|_{\beta=\beta_0}, \tag{7}$$

the high-order correction h is equal to

$$h = -\frac{f_0}{f_1}\left[1 + \frac{f_0 f_2}{2(f_1)^2} + \frac{f_0^2(3f_2^2 - f_1 f_3)}{6 f_1^4}\right]. \tag{8}$$

Now, the new more accurate approximation is equal to $\beta=\beta_0+h$. If necessary, other iterations can be done to improve accuracy.

B) Ortiz-Conde and coworkers

Another core model was proposed by Ortiz-Conde and coworkers, who developed a different solution for the case of intrinsic doping concentration in order to solve explicitly the surface potential equations [22], [23]. After some mathematical modifications the following expressions were obtained:

$$V_{gs} - V_{FB} = \varphi_S + \sqrt{\frac{2kTn_i\varepsilon_S}{C_{ox}^2}} e^{\frac{\varphi_S-\varphi_0}{2\varphi_T}} \sqrt{1 - e^{\frac{\varphi_0-\varphi_S}{\varphi_T}}}, \tag{9}$$

$$V_{gs} - V_{FB} = \varphi_S + \sqrt{\frac{2kTn_i\varepsilon_S}{C_{ox}^2}} e^{\frac{\varphi_S-\varphi_0}{2\varphi_T}} \sin(\varsigma) \tag{10}$$

and

$$\varphi_S(\varsigma) = V_{gs} - V_{FB} - -2\varphi_T LW\left[\frac{1}{C_{ox}\varphi_T}\sqrt{\frac{kTn_i\varepsilon_S}{2}}\, e^{\frac{V_{gs}-V_{FB}-V}{2\varphi_T}} \cdot \sin(\varsigma)\right], \tag{11}$$

where

$$\varsigma = \frac{t_S}{2L_{Di}} e^{\frac{\varphi_0 - V}{2\varphi_T}} \tag{12}$$

T is the temperature; V_{FB} is the flat-band voltage, n_i is the intrinsic doping concentration and LW is the Lambert function.

They proposed also an approximate solution for φ_0, considering that it changes from φ_S in subthreshold to $\varphi_{0\max} = V + 2\varphi_T \ln\left[\frac{\pi L_{Di}}{t_S}\right]$ in strong inversion, joining both values using a smoothing function. φ_0 is obtained from the following equations:

$$r = \left(At_{ox} + B\right)\left(\frac{C}{t_S} + D\right)e^{-E\,V} \tag{13}$$

$$U = \tfrac{1}{2}\left[V_{gs} - V_{FB} + (1+r)\varphi_{o\max}\right] \tag{14}$$

$$\varphi_0 = U - \sqrt{U^2 - (V_{gs} - V_{FB})\varphi_{0\max}} \tag{15}$$

where A= 0.0267 nm^{-1} ; B=0.0270; C=0.4526 nm; D= 0.0650; E= 3.2823 V^{-1}. Authors claimed that using this procedure, the error for the calculated surface potential is lower than 20 mV. This model was not further complemented.

C) Fossum and coworkers

Fossum and coworkers developed the charge-based compact model UFDG, which is a Poisson-Schrödinger solver for generic undoped DG MOSFETs [24], [25]. In this case the formalism for weak and strong inversion is separated. The moderate-inversion channel current, terminal charges and their voltage-derivatives are continuously defined by spline polynomial functions of gate voltage. This model presents some interesting characteristics, but it is now company propriety and is no longer open.

D) EPFL/UdS group

EPFL/University of Strasbourg group introduced a charge-based current model for symmetric undoped DG MOSFETs in correlation with the EKV formalism [26]. The relation between charges and applied voltages is obtained from the following implicit equation. This equation must be solved twice for charges at the source and at the drain.

$$v_g - v_{T0} - v_{ch} + \ln\left(\frac{q_{\text{int}}}{2}\right) = 4q_g + \ln(q_g) + \ln\left(1 + q_g \frac{C_{ox}}{C_S}\right), \tag{16}$$

where $v = \frac{V}{\varphi_T}$; $q = \frac{Q}{Qo}$; $Qo = 4C_{ox}\varphi_T$; $q_{\text{int}} = \frac{qn_i t_S}{Qo}$.

In the VHDL-AMS model implementation, [27], the numerical inversion algorithm used in order to solve this basic equation for two limiting cases: subthreshold and strong inversion is shown. Using a transition potential and a linearization function, authors claimed that charges are calculated 1000 times faster than by direct numerical calculation. In [28] some small geometry effects were considered. Presented validations, however, are very limited.

E) Fjeldly

A detailed analysis and modeling of the subthreshold and weak inversion regions was made using the conformal mapping techniques [29], [30]. A precise compact 2D model for lightly doped DG MOSFET was developed, which is very helpful in the case when the channel length is in the same order as silicon layer thickness, since in this case, the 2D behavior cannot be described by 1D model. This is the only model we have found, where this interesting solution method is used.

4. Modeling Doped DG MOSFETs

Different papers describe approaches in order to model the doped double-gate MOSFETs. In [31] a numerical solution for long channel devices is presented, where potentials and charges are calculated. However, this model was not further developed.

Another approach for long channel was done in [32]; however surface potential and drain current are calculated numerically.

A) EPFL/UdS group

EPFL/UdS group introduced in [33] the concept of equivalent-thickness of the silicon layer in order to consider the effect of the silicon layer doping. This concept features certain problems, since this equivalent thickness approaches zero at high concentrations. The same numerical algorithm as in [26] is used in this case for the surface potential calculation.

B) Chan and coworkers

In [34] this group presented, for long channel and constant mobility, a numerical solution for the potentials at the surface and at the center, solving two equations, one transcendental and another as function of *erf* and *erfi* functions, obtaining good coincidences for potentials and currents at different doping concentrations.

C) BSIM-MG

In 2012 the BSIM-MG model was adopted as industry standard. Two cases are considered: symmetric or common gate (CMG) and asymmetric gates (IMG). This model already considers the silicon layer doping concentration and short-channel effects.

In the case of symmetric gates and doped silicon layer, Poisson equation is solved using the perturbation method approach [35], [36]. The general equation has two terms: the first term attributed to inversion charges only and second term attributed to body doping N_a, where φ_F is the Fermi potential.

$$\frac{\partial^2 \varphi}{\partial x^2} = \frac{qn_i}{\varepsilon_S} e^{\frac{\varphi - \varphi_F - V}{\varphi_T}} + \frac{qN_a}{\varepsilon_S} . \tag{17}$$

The solution has also two terms, φ_1 considering only the first term, and φ_2 solving the second term as a perturbation. After defining a function of β, the sequence of calculation is the following:

$$f(\beta) = \ln(\beta) - \ln(\cos(\beta)) - \frac{V_{gfb} - V}{2\varphi_T} - \ln\left(\frac{t_S}{2}\sqrt{\frac{qn_i^2}{2\varepsilon_S \varphi_T N_a}}\right) + \mathrm{M}(\beta) = 0 \tag{18}$$

where:

$$M(\beta) = \frac{2C_S}{C_{ox}} \sqrt{\beta^2 \left(\frac{e^{\frac{\varphi_p}{\varphi_T}}}{\cos^2(\beta)} - 1 \right) + \frac{\varphi_p}{\varphi_T^2}\left(\varphi_p - 2\varphi_T \ln[\cos(\beta)]\right)} \tag{19}$$

and $V_{gfb} = V_{gs} - V_{fb} - V$.

Solution of (18) can be obtained by: 1) Newton-Rhaphson method; 2) table look approach; 3) analytical approximation with good initial solution β_0 and corrections of 3rd order h. This last method is the same as the one used by PSP [20], where $\beta=\beta_0+h$. If required, new iterations can be done.

After calculating β, the next steps are the calculations of $\varphi_0 \rightarrow \varphi_1 \rightarrow \varphi_2 \rightarrow \varphi_S$ using the following equations:

$$\varphi_0 = V + 2\varphi_T \left[\ln(\beta) - \ln\left(\frac{t_S}{2} \sqrt{\frac{qn_i^2}{2\varepsilon_S \varphi_T N_a}} \right) \right]; \tag{20}$$

$$\varphi_1(x,y) = \varphi_0(y) - 2\varphi_T \ln\left[\cos\left(\sqrt{\frac{qn_i^2}{2\varepsilon_S \varphi_T N_a} e^{\frac{\varphi_0 - V}{\varphi_T}}} \right) \right]; \tag{21}$$

$$\varphi_2(x,y) = \frac{2qn_i}{\varepsilon_S} \frac{e^{\frac{\varphi_F}{\varphi_T}}}{\alpha} \left(\frac{e^{x\sqrt{\alpha}} - 1}{2e^{\frac{x\sqrt{\alpha}}{2}}} \right); \tag{22}$$

where $\alpha = \frac{qn_i}{\varepsilon_S \varphi_T} e^{\frac{\varphi_1 - \varphi_F - V}{\varphi_T}}$.

Finally, the surface potential is calculated as:

$$\varphi_s(x,y) = \varphi_1(x,y) + \varphi_2(x,y) \tag{23}$$

The inversion charge as a function of surface potential is calculated as:

$$Q_{inv}(y) = C_{ox}(V_g - V_{fb} - \varphi_S(y)) - \sqrt{2q\varepsilon_S N_a \varphi_p}; \tag{24}$$

The drain current is calculated as:

$$I_d = 2\mu \frac{W}{L} \left[f(\varphi_{SS}) - f(\varphi_{SD}) \right], \tag{25}$$

where φ_{SS} and φ_{SD} are the surface potential at the source and at the drain, respectively, which are calculated from:

$$f(\varphi_s) = \frac{Q_{inv}^2}{2C_{ox}} + 2\varphi_T Q_{inv} - \varphi_T (5C_s \varphi_T + Q_b) \ln(5C_S \varphi_T + Q_b + Q_{inv}), \tag{26}$$

where $Q_b = qN_a t_s$.

BSIM-MG has 137 basic model parameters and 231 total parameters, requiring a special parameter extractor.

D) SDDGM

In 2008, an analytical and continuous compact model for short channel, symmetric and doped double-gate MOSFETs, the *Symmetric Doped Double-Gate MOSFET (SDDGM*) [37], [38], was presented. It considers a doped silicon layer in a wide range, from undoped to highly-doped and the mobile charge density is calculated using analytical expressions. The difference of potentials at the surface and at the center of the Si doped layer, ϕd, is defined by empirical expressions depending on the doping concentration N_a, silicon layer thickness t_s and dielectric thickness t_o. The transcendental equations are solved analytically, using Lambert function. The model includes variable mobility and short channel effects as velocity saturation, DIBL, V_T roll-off, channel length shortening and series resistance.

After the solution of the Poisson equation the surface electric field E_S is obtained as:

$$Es = \frac{1}{\varepsilon_s}\sqrt{\frac{2q_b C_s}{C_0}}\sqrt{\alpha}\sqrt{1+\frac{1-e^{-\alpha}}{\alpha}\cdot e^{\frac{\varphi_S-2\varphi_F-V}{\varphi_T}}}\ , \tag{27}$$

where $\alpha = \phi d / \varphi_T = (\varphi_S - \varphi_0) / \varphi_T$ is the normalized difference of potentials, $q_b = (qN_a t_s)/C_o\varphi_T$ is the modulus of the normalized total depletion charge in the silicon layer, ε_s is the silicon dielectric constant and $C_s = \varepsilon_s / t_s$ is the silicon layer capacitance per unit area.

Using detailed numerical calculations and simulations, it was found that the magnitude of ϕd can be expressed by empirical analytical expressions in the following three conditions:

1) Below threshold

$$\phi d_1 = \phi d_{BT} + \frac{19}{16}\varphi_T\left[\frac{e^{\frac{V_G-V_T-V}{\varphi_T}}}{1+e^{\frac{V_G-V_T-V}{\varphi_T}}}\right]; \tag{28}$$

2) Above threshold for $N_a<N_{amax}$

$$\phi d_{2a} = \phi d_{2aa} - (\phi d_{2aa} - \phi d_T)\cdot\frac{\left[1-\frac{V_G-V_T-V}{V_{GM}-V_T-V}\right]}{1-1.35\cdot(V_G-V_T-V)}; \tag{29}$$

where $\phi d_{2aa} = (\frac{\phi d_{BT}}{3} + \phi d_M - 0.042V)$, and

3) Above threshold, for $N_a \geq N_{amax}$:

$$\phi d_{2b} = \phi d_{2bb} - (\phi d_{2bb} - \phi d_T)\cdot\frac{\left[1-\frac{V_G-V_T-V}{V_{GM}-V_T-V}\right]}{1-0.5\cdot(V_G-V_T-V)}, \tag{30}$$

where $\phi d_{2bb} = (\phi d_{BT}/2 + \phi d_M - 0.042V)$ and N_{amax} corresponds to the doping concentration when the inversion at the center of the Si layer changes from strong to moderate inversion and the maximum difference of potentials ϕd_M is defined at the maximum gate voltage V_{GM} considered for these structures.

For V_{GM}= 2 V, ϕd_M is equal to:

$$\phi d_M = 0.197 - 0.047t_{ox} + 0.0045t_{ox}^2 + 0.00418t_s - 3x10^{-5}t_s^2\,. \tag{31}$$

Sewing (29) and (30) by means of the *tanh* function, the following expression was obtained:

$$\phi d_2 = \phi d_{2a}\frac{[1-\tanh QQ]}{2} + \phi d_{2b}\frac{[1+\tanh QQ]}{2}\ , \tag{32}$$

where $QQ = [10(\log N_a) - \log N_{a\max} - 0.5]$.

From (28) and (32) the complete expressions for ϕd and $\alpha = \phi d/\varphi_T$ are obtained:

$$\phi d = \phi d_1\frac{[1-\tanh[50\cdot(V_G-V_T-V)]]}{2} + \phi d_2\frac{[1+\tanh[50\cdot(V_G-V_T-V)]]}{2}\ . \tag{33}$$

Figure 2 shows the validation of (33) for different drain voltages and doping concentrations.

The surface potential is calculated analytically using the following expressions:
In the subthreshold region:

$$\varphi_{sbt} = V_G - V_{FB} - \varphi_T \frac{q_b}{2} - \varphi_T \cdot LW\left[\frac{q_b}{4} e^{\frac{V_G - V_{FB} - 2\varphi_F}{\varphi_T} - \frac{qb}{2}}\right], \tag{34}$$

In the above threshold region:

$$\varphi_{sat} = V_G - V_{FB} - 2\varphi_T \cdot LW\left[\frac{1}{2}\sqrt{\frac{2q_b C_s}{C_o}}\sqrt{1-e^{-\alpha}}\, e^{\frac{V_G - V_{FB} - 2\varphi_T - V}{2\varphi_T}}\right], \tag{35}$$

and the continuous value of surface potential in all regions is calculated as:

$$\varphi_s = \varphi_{sbt}\,\tfrac{1}{2}[1-\tanh[20\cdot(V_G - V_T)]] + \varphi_{sat}\,\tfrac{1}{2}[1+\tanh[20\cdot(V_G - V_T)]] \tag{36}$$

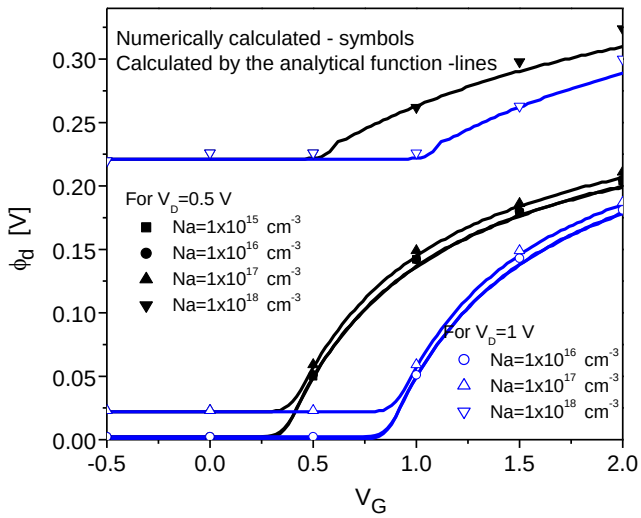

Fig. 2 Difference of potential at the surface and at the center of the silicon layer, calculated numerically and analytically for different drain voltages and doping concentrations

Mobile charge at the surface, at both interfaces, normalized to $C_{ox}\varphi_T$ is equal to:

$$q_n = \sqrt{\frac{2q_b C_S}{C_{ox}}}\,\sqrt{\alpha}\sqrt{1+\frac{1-e^{-\alpha}}{\alpha}\cdot e^{\frac{\varphi_S - 2\varphi_F - V}{\varphi_T}}} - \frac{q_b}{2} \tag{37}$$

and the relation between the variation of the normalized mobile charge q_n and the voltage along the channel V, from the charge control model, is equal to:

$$dV = \varphi_T\left(1+\frac{1}{q_n}+\frac{1}{q_n+q_b}\right) \tag{38}$$

Replacing (29) and (30) in the usual drain current integral:

$$I_{DS} = 2\frac{W}{L}\mu C_o \varphi_T \int_{V_S}^{V_D} q_n(V)\, dV \cdot \tag{39}$$

The drain current is calculated by the following expression:

$$I_{DS} = 2\frac{W}{L}\mu C_{ox}\varphi^2 \cdot \left[\frac{q_{ns}{}^2 - q_{nd}{}^2}{2} + 2(q_{ns} - q_{nd}) - q_b \ln\left(\frac{q_{ns} + q_b}{q_{nd} + q_b}\right)\right]. \tag{40}$$

After including variable mobility, short channel effects, and series resistance in (40) the drain current equation is expressed as:

$$I_{DS} = \frac{\left(2\frac{W}{L}C_{ox}\mu_S \phi t^2\right)\cdot fqq}{\left(1 - \frac{\Delta L}{L}\right)\cdot fcorr} \tag{41}$$

where

$$fqq = \left\{\frac{1}{2}(q_{ns}^2 - q_{nd}^2) + \left[2(q_{ns} - q_{nd}) - q_b \ln\left(\frac{q_{ns} + q_b}{q_{nd} + q_b}\right)\right]^n\right\}, \tag{42}$$

$$fcorr = \left\{\sqrt{\left(1 + \left(\frac{\mu_S V_{Def}}{v_{sat} L}\right)^2\right)} + \left[2\frac{W}{L}C_{ox}\mu_S \cdot R \cdot \left|V_{GT} - \frac{1}{2} + \frac{C_S}{C_{ox} + C_S}\cdot V_{Def}\right|\right]\right\} \tag{43}$$

and the surface variable mobility is equal to:

$$\mu_S = \frac{\mu o}{1 + \left(\frac{\overline{E}}{E_1}\right)^{P1} + \left(\frac{\overline{E}}{E_2}\right)^{P2}}. \tag{44}$$

E_1, E_2, $P1$, $P2$ are adjusting parameters. A more detailed description can be found in [38]. This model has 7 technological parameters and 11 adjusting parameters, including 6 for mobility. These parameters can be extracted by optimization methods from measured/simulated I-V characteristics. A simple extraction procedure was developed in IC-CAP [39].

In all cases, validation of SDDGM for the core model gave an excellent coincidence between simulated and modeled characteristics without any adjusting parameter [37]. In addition, a very extensive validation of the method was performed using different SOI FinFET transistors with poly-Si gate and highly doped silicon layer, as well as for metal gate with low doped silicon layer [37]**.** Validation versus temperature and symmetry was presented in [40].

SDDGM was implemented in Verilog-A [41] and introduced in circuits simulators SmartSPICE and SMASH. Circuit simulations in SmartSPICE using N-channel and P-channel transistors are presented in [42]-[44]. Application of SDDGM to nanometric Bulk FinFET is extensively shown in [45], for different dimensions, channel conductivity and

temperatures, where characteristics obtained in the circuit simulator reproduce well measured characteristics.

SCE as threshold voltage roll-off, DIBL, channel shortening and series resistance are described in detail in [38].

An important gate leakage current effect in short channel nanometric FinFETs was also modeled and incorporated into SDDGM. Both single high-k dielectric and dielectric stack cases were considered and validated in [46], [47]. To model the gate leakage current, additional parameters are required: 3 for direct tunneling; 3 for trap-assisted tunneling; 4 for direct tunneling assisted by electron-hole pair generation process and 2 for GIDL.

Another interesting application of SDDGM was done in the field of microwave transistors. A high-frequency compact analytical noise model for DG MOSFETs was obtained using the SDDGM DC model [48] and the compact small-signal model for RF FinFETs, where the high frequency equivalent circuit model parameters were extracted from de SDDGM DC model [49], [50].

5. SDDGM EXAMPLES

Figure 3 demonstrates an excellent agreement between the measured and modeled with SDDGM FinFET characteristics. The transistor parameters were: channel length of 40 nm; fin width of 12 nm; fin height of 60 nm; 480 fins in parallel for a total channel width of 63.36 μm; doping concentration of 10^{15} cm^{-3} and EOT of 1.8 nm. Transfer characteristics for V_D= 0.05 and 1.2 V in normal and semilog scales are shown. The leakage current due to GIDL effect was included in the modeled characteristic at V_D = 1.2V.

Transconductance curves in linear and saturation regimes are shown in Fig. 4, where a good agreement is observed for both operations regimes.

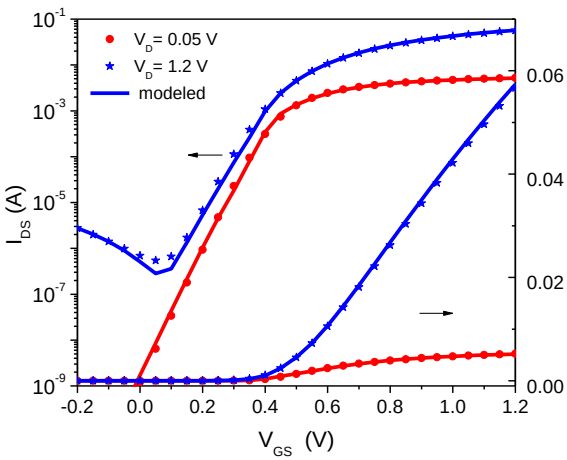

Fig. 3 Transfer characteristics of FinFET with L=40 nm at V_D=0.05 and 1.2 V

measurements up to 110 GHz, where the extraction frequency band was from 5 to 20 GHz. The comparison with modeled capacitances is shown in Fig 5, providing a reasonable coincidence for that type of high frequency parameters.

Circuit simulation with FinFETs using the SDDGM implemented in the circuit simulator SmartSPICE was reported in [43]. Fig 6 shows the schematic of the inverting Miller OpAmp. This analog block was fabricated and measured by G. Knoblingerl et al. [51]. FinFETs and circuit have the following parameters: L= 250 nm; H_{FIN}= 88 nm; W_{FIN} = 55 nm; the circuit contains a resistance R=100 kΩ and a capacitor C= 2 pF. The total transistors channel width is defined by the number of fins shown in Table 1.

Measured [51] and simulated [43] frequency response of the OpAmp are shown in Fig. 7, observing a very good agreement between both characteristics, describing the whole transistor behavior.

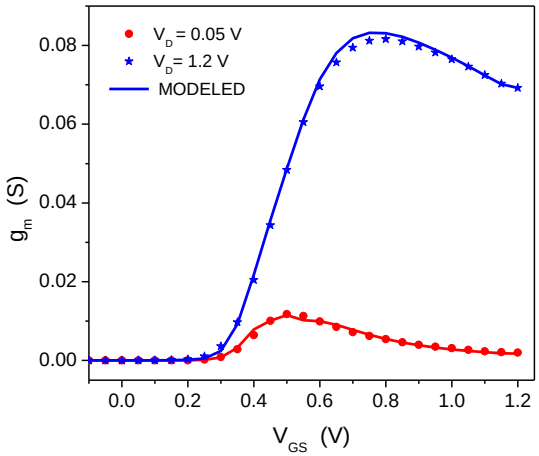

Fig. 4 Transconductance of FinFET with L= 40 nm at V_D = 0.05 and 1.2 V

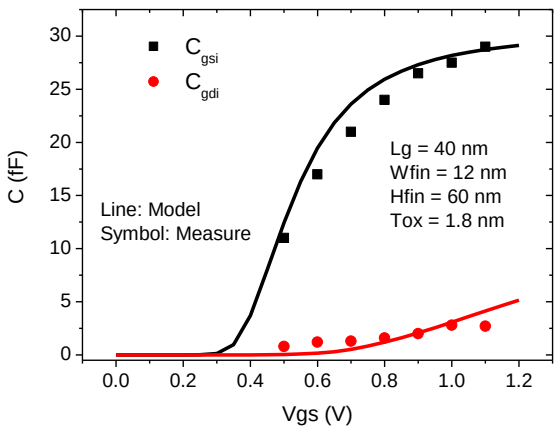

Fig. 5 FinFET intrinsic capacitances Cgs and Cgd, measured in the frequency band from 5 to 20 GHz and modeled at V_D= 1 V

Table 1 Number of fins for each transistor in Fig. 6

transistor	type	fins
P1	P	8
P2	P	8
P3	P	128
M1	N	8
M2	N	8
M3	N	8
M4	N	64
M5	N	8

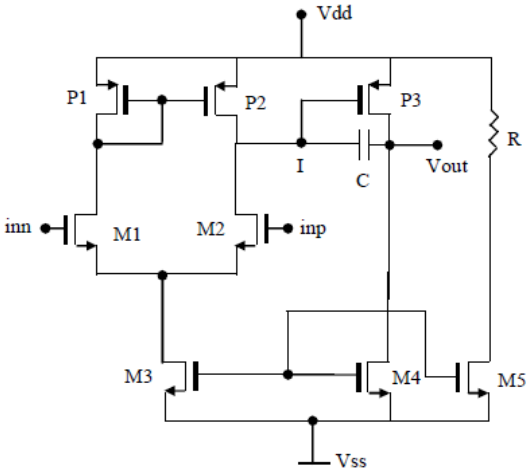

Fig. 6 Schematics of OpAmp circuit with FinFETs

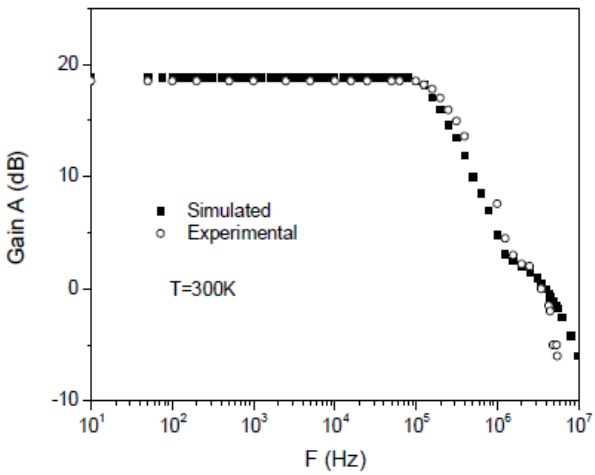

Fig. 7 Frequency response of inverting Miller OpAmp: measured and simulated

6. CONCLUSIONS

In the last years, multigate devices are being intensively studied in order to obtain new MOSFET structures allowing the reduction of transistor dimensions, while maintaining high performance. FinFET devices, both SOI and Bulk, with two and three gates seem to be suitable devices for a new generation of MOSFETs, especially for analog applications. Among compact models developed for representing their behavior, we have summarized the fundamental bases which are the most significant from our point of view. We started with the first approaches that considered the limiting cases of either undoped or highly doped silicon layer. Then, the Symmetric Doped Double-Gate Model, SDDGM, which considers a wide range of channel doping, SCE, variable mobility and effects of leakage currents, was explained in more details. Examples of its application to transistor and circuit simulation with both SOI and bulk DG FinFETs are either shown or referenced, including the one related to microwave transistors.

Acknowledgement: *This work was supported by CONACYT project 127978, by the Spanish Ministry of Science and Innovation under project TEC2011-28357-C02-01 and ICREA Academia Award and by FNRS(Belgium) and COMON, SINANO and Nanosil EU projects. Authors acknowledge Imec and J.-P. Raskin for provided devices information and Pascal Simon for his support with RF setup/measurements.*

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