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AN ANALYTICAL SUBTHRESHOLD CURRENT/SWING MODEL FOR JUNCTIONLESS CYLINDRICAL NANOWIRE FETS (JLCNFETS)

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Abstract. *Based on the parabolic potential approach (PPA), scaling theory, and drift-diffusion approach (DDA) with effective band gap widening (BGW), we propose an analytical subthreshold current/swing model for junctionless (JL) cylindrical nanowire FETs (JLCNFETs). The work indicates that the electron density of Q_m that is induced by the current factor β, minimum central potential $\Phi_{c,min}$ and equivalent quantum potential Φ_{QM} is used to determine the subthreshold current/swing for JLCNFET. Unlike the junction-based (JB) cylindrical nanowire FETs (JBCNFETs), the subthreshold current for JLCNFET is not linearly proportional to the silicon diameter, but linearly proportional to the current factor β due to the depletion-typed operation. Apart from short-channel effects (SCEs), the quantum-mechanics effects (QMEs) are included in the model by accounting for the effective BGW, which decreases the electron density in the subthreshold regime and reduces the subthreshold current consequently. Band-to-band tunneling (BTBT) that impacts the subthreshold current is also discussed in the end of the paper. The model explicitly shows how the bulk doping density, drain bias, channel length, oxide thickness, gate workfunction, and silicon film diameter affect the subthreshold current/swing. The model is verified by its calculated results matching well with the data simulated from the three-dimensional device simulator and can be used to investigate the subthreshold current/swing for JLCNFET.*

Key words: *Scaling theory, Parabolic potential approach, Subthreshold current, Subthreshold swing, Drift-diffusion approach, Effective bad gap widening, Short-channel effects, Quantum-mechanics effects, BTBT, JLCNFET*

1. INTRODUCTION

It is reported that the non-planar FETs of double-gate (DG), triple-gate (TG), and surrounding-gate (SRG) FETs are recognized as emerging devices for the high-performance (HP) application circuits [1]. Although these non-planar devices are superior over con-

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ventional planar devices in respect of suppressing the SCEs, the formation of ultra-sharp and super-shallow source/drain junctions to suppress SCEs still stringently constrain the doping techniques and thermal budget. To overcome these problems, the junctionless (JL) FETs have been proposed [2]-[4].

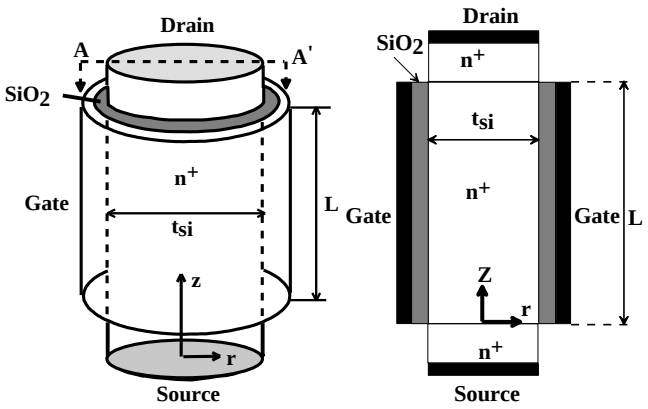

Fig. 1 Schematic of junctionless cylindrical, nanowire FET (JLCNFET): (a) three-dimensional device structure, (b) with cut plane along A-A', two-dimensional device structure is used to derive the model. For simplicity, both the source and drain regions are assumed to be zero thicknesses.

For JL devices, the doping concentration is constant through the entire device including source, channel, and drain. The absence of doping concentration gradient between source/drain and channel eliminates the problem of sharp doping profile formation and saves the thermal budget. For power saving issue, the subthreshold current/swing plays a very important role in the low operating power (LOP) circuits [5], [6]. For further exploitation and use of the JL FETs in the subthreshold regime, it is mandatory to develop a feasible, physics-based subthreshold current/swing model. Recently, several studies have reported the analytical current models for JL multiple-gate (MG) FETs (JLMGFETs). However, all of these studies only put a focus on the current models for long-channel JLCNFETs [7] and long-channel/short-channel JL double-gate FETs (JLDGFETs) [8], [9]. None of these studies reported the short-channel subthreshold current/swing model for JLCNFETs. In this paper, based on the PPA, the scaling theory, and the DDA with effective BGW, an analytical subthreshold current/swing model for JLCNFET is successfully developed. The model accounting for both SCEs and QMEs can precisely predict the subthreshold current/swing over a wide range of device parameters. The model not only thoroughly investigates how the device parameters take an effect on the subthreshold current/swing, but also provides the basic designing guidance for JLCNFET. The paper is organized as follows: section 2 addresses how to obtain the short-channel potential distribution through quasi-2D PPA in solving 2-D Poisson's equation. The channel potential will comprise both the surface and central potentials in a single equation, which helps to determine the subthreshold current by the parameter transformation. Section 3 is devoted to determine the minimum central potential in the

channel based on the quasi-2D scaling theory, where the volume conduction mechanism (VCM) is included. In section 4, we develop the subthreshold current model for both short-channel and long-channel devices by the DDA with the effective BGW to account for QMEs, which hence decreases the electron density in the subthreshold regime and reduces the subthreshold current. By considering both SCEs and QMEs, the electron density of Q_m is developed to monitor the subthreshold current. In section 5, we derive the subthreshold swing model including both the short-channel and long-channel JLCNFETs. Section 6 demonstrates how the device parameters such as the silicon film diameter, gate oxide thickness, gate workfunction, drain bias, and doping density affect the subthreshold current/swing. Meanwhile, a comparison between JLDGFET and JLCNFET is made for the subthreshold swing. The BTBT effects that impact the subthreshold current are also discussed in the end of this section. Finally, we draw some conclusions in section 7.

2. PARABOLIC POTENTIAL APPROACH (PPA) FOR SHORT-CHANNEL POTENTIAL DERIVATION

Fig. 1(a) shows the three-dimensional device structure for JLCNFET. With cut-plane along AA', Fig. 1(b) shows the two-dimensional device structure to derive the model. The z-axis and r-axis are parallel and vertical to the channel direction, respectively. Since JLCNFET is operating in the subthreshold regime, the free carrier concentration is much less than the impurity density so that the net charge density can be dominated by the donor concentration. Therefore, the channel potential $\Phi(r,z)$ should satisfy the following two-dimensional Poisson's equation:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\Phi(r,z)\right)+\frac{\partial^2\Phi(r,z)}{\partial z^2}=\frac{-qN_d}{\varepsilon_{si}} \tag{1}$$

where N_d is the bulk doping density, ε_{si} is the silicon dielectric permittivity, and q is the unit of electric charge. By using the PPA to solve the two-dimensional Poisson's equation, the potential vertical to the channel direction can be assumed by $\Phi(r,z)=C_1(z)+C_2(z)r+C_3(z)r^2$ that will satisfy the following boundary conditions [10]:

$$\begin{cases}\Phi(0,z)=C_1(z)=\Phi_c(z)\\ \dfrac{\partial\Phi(r,z)}{\partial r}\Big|_{r=\frac{t_{si}}{2}}=\dfrac{C_{ox}}{C_{si}t_{si}}\left(V_{gs}-V_{fb}-\Phi_s(z)\right)\\ \dfrac{\partial\Phi(r)}{\partial r}\Big|_{r=0}=0\end{cases} \tag{2}$$

where $\Phi_c(z)$ is the central potential, C_{ox} is the effective oxide capacitance per unit area, C_{si} is the bulk silicon capacitance per unit area, $\Phi_s(z)$ is the surface potential, V_{gs} is the gate voltage, and V_{fb} is the flat-band voltage that can be determined by the workfunction difference between the silicon film and the gate electrode. By using (2) to solve the coefficients of $C_1(z)$, $C_2(z)$, and $C_3(z)$, we can find the channel potential as a combination of the surface and central potentials. It yields

$$\Phi(r,z)=\Phi_C(z)+\frac{C_{ox}}{C_{si}t_{si}^{\ 2}}\left(V_{gs}-V_{fb}-\Phi_S(z)\right)r^2 \tag{3}$$

where

$$\Phi_S(z)=\frac{4C_{si}\Phi_C(z)+C_{ox}\left(V_{gs}-V_{fb}\right)}{4C_{si}+C_{ox}} \tag{4}$$

with

$$\begin{cases} C_{ox}=\dfrac{\varepsilon_{ox}}{\dfrac{t_{si}}{2}\ln(1+\dfrac{2t_{ox}}{t_{si}})} \\ C_{si}=\dfrac{\varepsilon_{si}}{t_{si}} \end{cases} \tag{5}$$

3. Scaling Theory in Bulk Conduction Mode (BCM) to Determine the Minimum Central Channel Potential

By accounting for bulk conduction mechanism (BCM) for JLCNFET and following the previously developed scaling theory for junction-based (JB) cylindrical, surrounding-gate (JBCSG) MOSFET [11], the central potential for JLCNFET should satisfy the following scaling equation:

$$\frac{d^2\Phi_C(z)}{dz^2}-\frac{1}{\lambda_C^{\ 2}}(\Phi_C(z)-\phi_C)=0 \tag{6}$$

with

$$\frac{1}{\lambda_C^{\ 2}}=\frac{16C_{OX}}{4t_{si}\varepsilon_{si}+C_{OX}t_{si}^{\ 2}} \tag{7}$$

and

$$\phi_C=V_{gs}-V_{fb}+\frac{qN_dt_{si}}{4C_{OX}}+\frac{qN_dt_{si}}{16C_{si}} \tag{8}$$

where λ_C is the scaling length for JLCNFET with BCM, ϕ_C is the central potential for the long-channel device. By solving the ordinary differential equation, the general solution of (6) can be expressed as

$$\Phi_C(z)=ae^{\frac{1}{\lambda_C}z}+be^{\frac{-1}{\lambda_C}z}+\phi_C \tag{9}$$

The coefficients of a and b in (9) can be determined by using the boundary conditions at the source/silicon junction (i.e., $\Phi_C(z=0)=V_{bi}$) and the drain/silicon junction (i.e., $\Phi_C(z=L)=V_{bi}+V_{ds}$). They are obtained as follows:

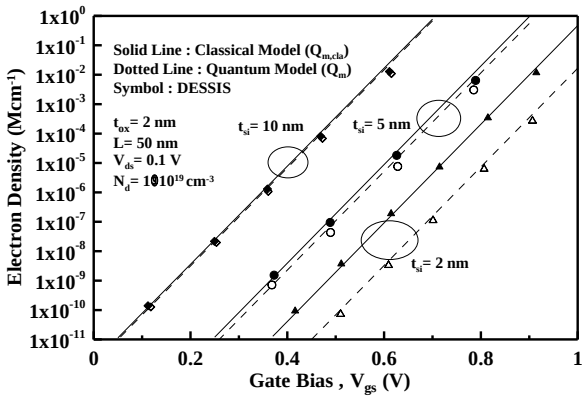

Fig. 2 Quantum-mechanics and classical electron charge densities in subthreshold operation regime for t_{si} = 2nm, 5nm and 10 nm

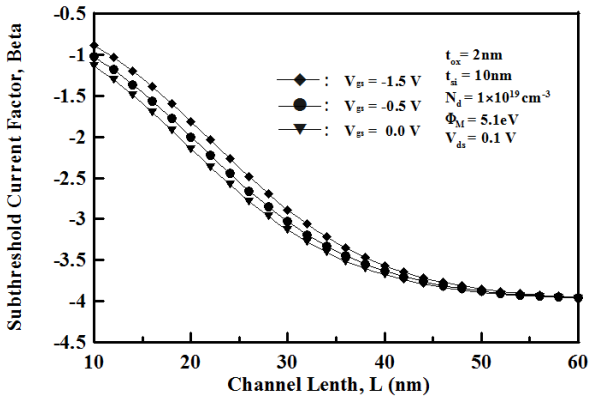

Fig. 3 Subthreshold current factor β versus channel length for different gate voltages

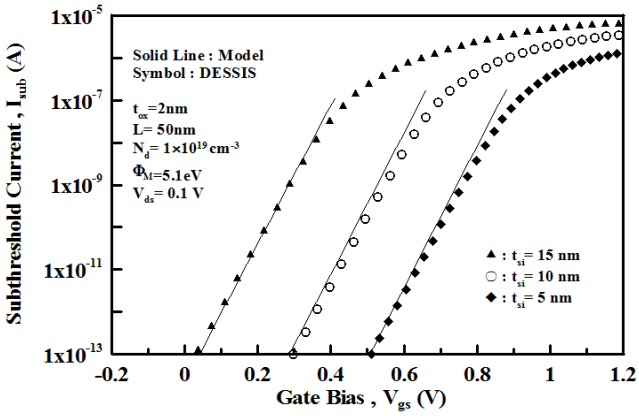

Fig. 4 Subthreshold current versus gate bias for different gate oxide thicknesses

$$\begin{cases} a = \dfrac{e^{-L/\lambda_C} - 1}{2\sinh(L/\lambda_C)} V_{gs} + \dfrac{V_{ds} - \omega(e^{-L/\lambda_C} - 1)}{2\sinh(L/\lambda_C)} \\ b = \dfrac{1 - e^{L/\lambda_C}}{2\sinh(L/\lambda_C)} V_{gs} - \dfrac{V_{ds} - \omega(e^{L/\lambda_C} - 1)}{2\sinh(L/\lambda_C)} \end{cases} \tag{10}$$

with

$$\omega = V_{fb} + V_{bi} - \frac{qN_d t_{si}}{4C_{OX}} - \frac{qN_d t_{si}}{16C_{si}} \tag{11}$$

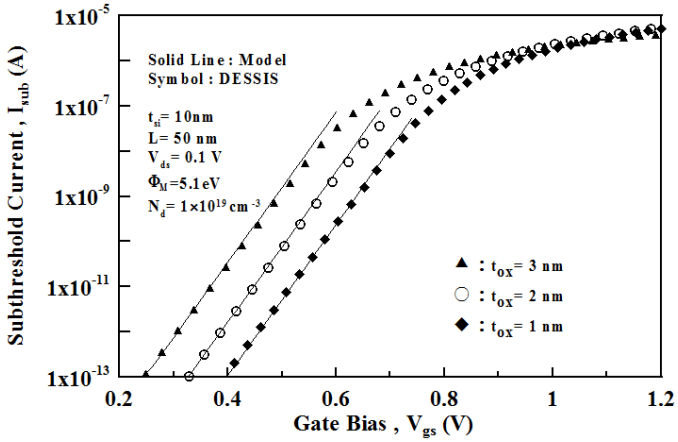

Fig. 5 Subthreshold current versus gate bias for different gate oxide thicknesses

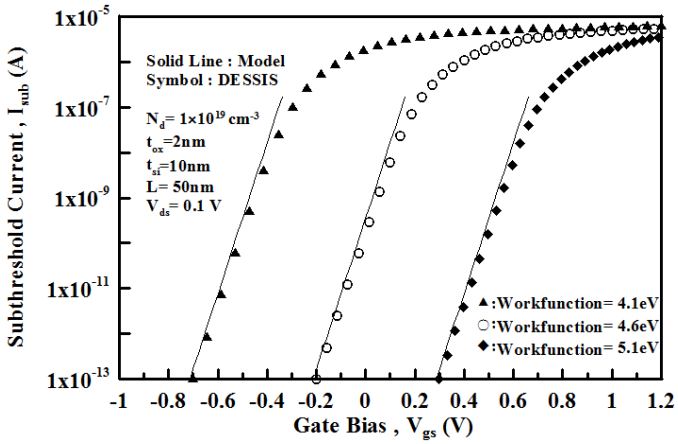

Fig. 6 Subthreshold current versus gate bias for different workfunctions

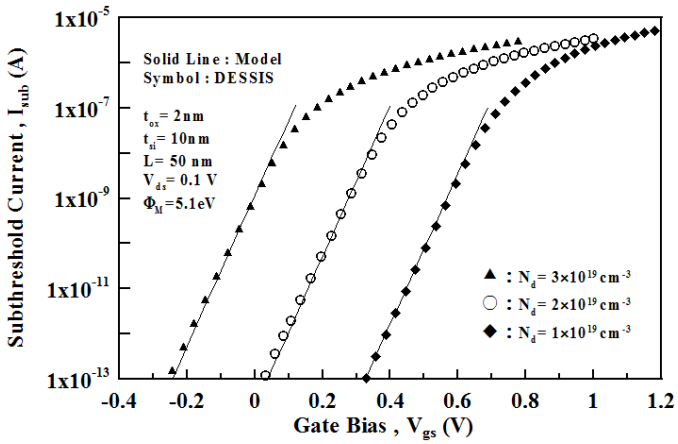

Fig. 7 Subthreshold current versus gate bias for different silicon doping densities

Due to the homogeneous doping density between source/drain and channel regions, the built-in potential V_{bi} in (11) can be negligible. Because the arithmetic mean is larger than or equal to the geometric mean, the minimum central potential in (9) can be obtained as

$$\Phi_{C,\min} = 2\sqrt{ab} + \phi_C \tag{12}$$

with

$$Z_{\min} = \frac{L}{2} - \frac{\lambda_C}{2}\ln(\frac{b}{a}) \tag{13}$$

where Z_{min} is the so-called virtual cathode point (VCP) that indicates the location for the leakiest path in the subthreshold region. By substituting (12) into (4), the minimum surface potential for JLCNFET can be expressed as

$$\Phi_{S,\min} = \frac{4C_{si}\Phi_{C,\min} + C_{ox}(V_{gs} - V_{fb})}{4C_{si} + C_{ox}} \tag{14}$$

With a combination for both the minimum surface and central potentials, the minimum channel potential in (3) can be found as

$$\Phi_{\min}(r) = \Phi_{C,\min} + \frac{C_{ox}}{C_{si}t_{si}^{\ 2}}(V_{gs} - V_{fb} - \Phi_{S,\min})r^2 \tag{15}$$

The minimum central potential linking to the minimum surface potential to express the minimum channel potential helps to solve the integration for the subthreshold current, which will be demonstrated in the next section.

4. DRIFT-DIFFUSION APPROACH (DDA) WITH EFFECTIVE BAND GAP WIDENING (BGW) FOR SUBTHRESHOLD CURRENT DERIVATION

A) Short-channel case:

With the minimum channel potential of (15), we can proceed to derive the subthreshold current. Since the current density for JLCNFET flows predominantly in the z direction (from source to drain), the electron quasi-Fermi potential Φ_n is essentially constant in the r-direction and can be assumed as only function of z. By using the DDA with effective BGW [12], [13], the current density (both drift and diffusion terms) together with the electron carrier density $n_{i,\min}$ at the virtual cathode point (VCP) [14], [15] can be written as

$$J_n(r,z) = q\mu n_{i,\min}(r,z)\frac{d\Phi_n(z)}{dz} \tag{16}$$

with

$$n_{i,\min}(r,z) = n_i \exp(\frac{\Phi_{\min}(r) - \Phi_n(z) + \Phi_f - \Phi_{QM}}{V_T}) \tag{17}$$

where $n_{i,\min}(r,z)$ is the electron density at VCP by considering the effective BGW [16], n_i is the intrinsic carrier density, V_T=KT/q is the thermal voltage, Φ_F is bulk potential (=$V_T\ln(N_d/n_i)$), $\Phi_n(z)$ is the electron quasi-Fermi potential, and Φ_{QM} is the so-called equivalent quantum potential (i.e., the equivalently increased classical channel potential) caused by the effective BGW that results from the QMEs and can be defined by [17]:

$$\begin{cases} E_{G,QM} = E_{G,CL} + \Delta E_G \\ \Delta E_G = \dfrac{\pi^2\hbar^2}{2m^* t_{si}^{\,2}} = q\Phi_{QM} \end{cases} \tag{18}$$

where $E_{G,QM}$ is the classical band gap, $E_{G,CL}$ is the quantum-mechanics band gap, and Φ_{QM} is the equivalently increased classical channel potential when QMEs induce the effective BGW. As JLCNFET with a very thin silicon film operates in the subthreshold regime, QMEs will effectively increase the classical band gap, which is the so-called effective BGW. The increased value of the classical bang gap ΔE_G induced by BGW generates from the lowest split subband of the conduction band when QMEs are initiated by the very thin silicon film of the device. By integrating (16) in both the r and θ directions, the subthreshold current along z direction for JLCNFET can be obtained as

$$I_{sub}(z) = \int_0^{\frac{t_{si}}{2}}\int_0^{2\pi} q\mu n_i \exp(\frac{\Phi_{\min}(r) - \Phi_n(z) + \Phi_F - \Phi_{QM}}{V_T})\frac{d\Phi_n(z)}{dz} r\,d\theta\,dr \tag{19}$$

Since the current is constant along the channel direction, integration of (19) with respect to z from 0 to L will yield

$$I_{sub} = \frac{q\mu V_T[1-\exp(-\frac{V_{ds}}{V_T})]\exp(\frac{-\Phi_{QM}}{V_T})\int_0^{\frac{t_{si}}{2}}\int_0^{2\pi} N_d \exp(\frac{\Phi_{\min}(r)}{V_T}) r\,d\theta\,dr}{L} \tag{20}$$

where $\Phi_n(z=0)=0$, $\Phi_n(z=L)=V_{ds}$, μ is the constant electron mobility ($\mu = 1417 cm^2/Vs$), and V_{ds} is the drain voltage. By using (15) and the change of variables (i.e., $dr \to d\Phi$), the subthreshold current in (20) can be solved as

$$\begin{aligned} I_{sub} &= \frac{q\mu\varepsilon_{si}V_T^{\,2}\pi t_{si}N_d \exp(\frac{-\Phi_{QM}}{V_T})[1-\exp(-\frac{V_{ds}}{V_T})][\exp(\frac{\Phi_{S,\min}}{V_T})-\exp(\frac{\Phi_{C,\min}}{V_T})]}{LC_{ox}\left(V_{gs}-V_{fb}-\Phi_{S,\min}\right)} \\ &= \frac{\mu\varepsilon_{si}V_T^{\,2}\beta\pi[1-\exp(-\frac{V_{ds}}{V_T})]\exp(\frac{-\Phi_{QM}}{V_T})[\exp(\frac{\Phi_{S,\min}}{V_T})-\exp(\frac{\Phi_{C,\min}}{V_T})]}{L} \\ &= \frac{\mu V_T Q_m[1-\exp(-\frac{V_{ds}}{V_T})]\exp(\frac{-\Phi_{QM}}{V_T})}{L} \end{aligned} \tag{21}$$

with

$$\beta = \frac{qN_d t_{si}}{C_{ox}(V_{gs}-V_{fb}-\Phi_{S,\min})} \tag{21a}$$

$$Q_m = Q_{m,cla}\exp(\frac{-\Phi_{QM}}{V_T}) \tag{21b}$$

$$Q_{m,cla} = \beta\pi\varepsilon_{si}V_T[\exp(\frac{\Phi_{S,\min}}{V_T})-\exp(\frac{\Phi_{C,\min}}{V_T})] \tag{21c}$$

where β is defined as a subthreshold current factor that determines the subthreshold current for JLCNFET operating in the subthreshold region. By considering SCEs and QMEs, Q_m is the electron density per unit length in the subthreshold region. By considering SCEs only, $Q_{m,cla}$ is the electron density of classical device in the subthreshold region. Substituting (12) and (14) into (21) will lead to the subthreshold current for JLCNFET. Because JLCNFET is usually a highly doped device (for instance, the channel doping density for JLCNFET is usually $\geq 10^{19} cm^{-3}$ [18], [19]), the central potential will be larger than the surface potential, which results in

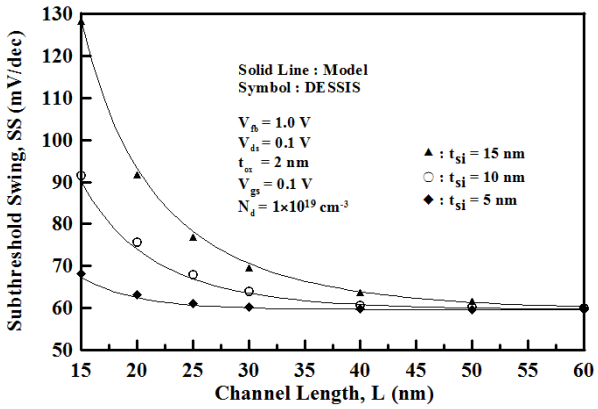

Fig. 8 Subthreshold swing versus channel length for different silicon film diameters

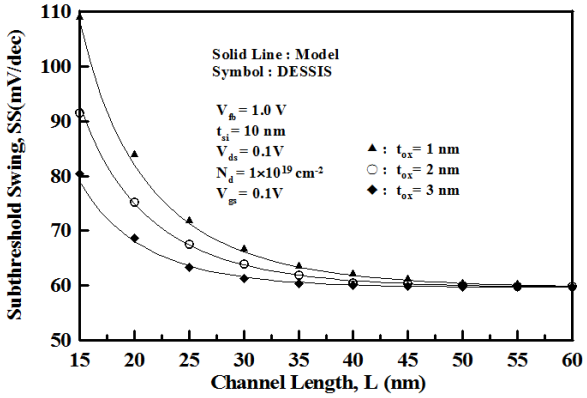

Fig. 9 Subthreshold swing versus channel length for different gate oxide thicknesses

$\exp(\frac{\Phi_{C,\min}}{V_T}) >> \exp(\frac{\Phi_{S,\min}}{V_T})$. Hence, the equation of (21) becomes

$$I_{sub} = \frac{-\mu\varepsilon_{si}V_T{}^2\beta\pi[1-\exp(-\frac{V_{ds}}{V_T})]\exp(\frac{\Phi_{C,\min}}{V_T})\exp(\frac{-\Phi_{QM}}{V_T})}{L} = \frac{-\mu V_T Q_m[1-\exp(-\frac{V_{ds}}{V_T})]}{L} \quad (22a)$$

with

$$Q_m = Q_{m,cla}\exp(\frac{-\Phi_{QM}}{V_T}) \quad (22b)$$

$$Q_{m,cla} = -\beta\pi\varepsilon_{si}V_T\exp(\frac{\Phi_{C,\min}}{V_T}) \quad (22c)$$

Q_m in (22b) is uniquely determined by the subthreshold current factor β, equivalent quantum potential Φ_{QM}, and minimum central potential $\Phi_{C,min}$. The dependence of β on the channel length will be demonstrated in Fig. 3.

B) Long-channel case:

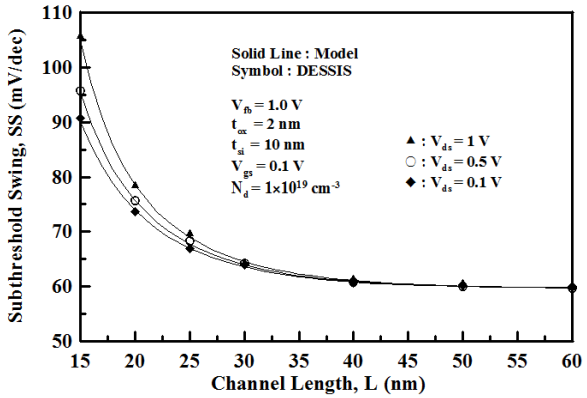

Fig. 10 Subthreshold swing versus channel length for different drain biases

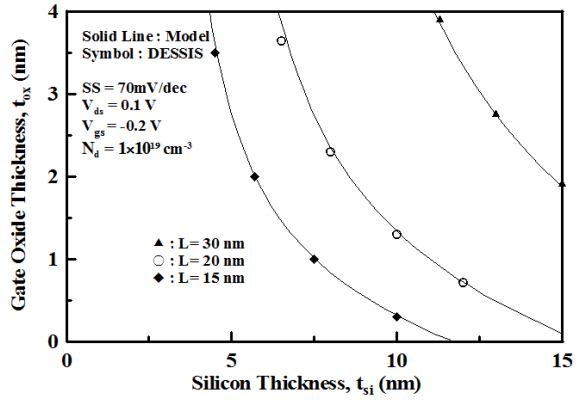

Fig. 11 The designing space for both of the silicon diameter and the gate oxide thickness. The maximum allowable subthreshold swing is 70mV/dec

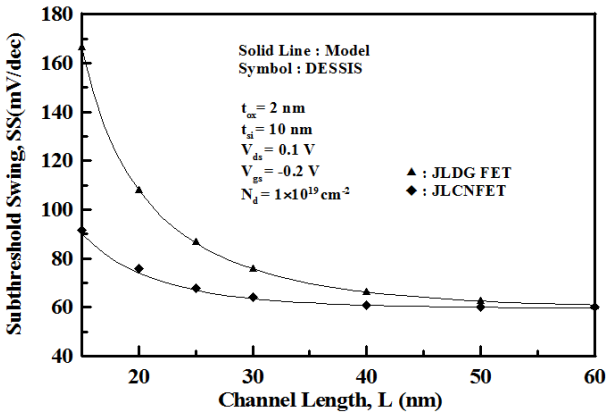

Fig. 12 The comparison of the subthreshold swing between JLCNFET and JLDGFET

For a long-channel device, the coefficient of a in (10) approaches zero (i.e., $a \approx 0$ in (10)), the minimum central potential in (12) will be given by $\Phi_{C,\min} = \phi_C$. We use the minimum central potential $\Phi_{C,\min} = \phi_C$ and equation of (14) to derive the long-channel minimum surface potential. It yields

$$\Phi_{S,\min} = \phi_S = \frac{4C_{si}\phi_C + C_{ox}(V_{gs} - V_{fb})}{4C_{si} + C_{ox}} \tag{23}$$

where ϕ_S and ϕ_C are the long-channel minimum surface and central potentials for JLCNFET. By substituting (8) and (23) into (21) and (22a), the long-channel subthreshold current for JLCNFET can be obtained as

$$
\begin{aligned}
I_{sub} &= \frac{\mu\varepsilon_{si}V_T{}^2\beta\pi[1-\exp(-\frac{V_{ds}}{V_T})]\left[\exp(\frac{\phi_S}{V_T})-\exp(\frac{\phi_C}{V_T})\right]\exp(\frac{-\Phi_{QM}}{V_T})}{L} \\
&\approx \frac{-\mu\varepsilon_{si}V_T{}^2\beta\pi[1-\exp(-\frac{V_{ds}}{V_T})]\exp(\frac{\phi_C}{V_T})\exp(\frac{-\Phi_{QM}}{V_T})}{L} \\
&\approx \frac{-\mu\varepsilon_{si}V_T{}^2\beta\pi[1-\exp(-\frac{V_{ds}}{V_T})]\exp(\frac{V_{gs}-V_{th}}{V_T})\exp(\frac{-\Phi_{QM}}{V_T})}{L} \\
&\approx \frac{-\mu V_T Q_m[1-\exp(-\frac{V_{ds}}{V_T})]}{L}
\end{aligned}
\tag{24}
$$

with

$$V_{th} = V_{fb} - \frac{qN_d t_{si}}{4C_{OX}} - \frac{qN_d t_{si}}{16C_{si}} \tag{25a}$$

$$Q_m = Q_{m,cla}\exp(\frac{-\Phi_{QM}}{V_T}) \tag{25b}$$

$$Q_{m,cla} = -\beta\pi\varepsilon_{si}V_T\exp(\frac{V_{gs}-V_{th}}{V_T}) \tag{25c}$$

whereV_{th} is the long-channel classical threshold voltage for JLCNFET. It is worthy to point out that (25c) is similar with the formula [7] due to the following points: 1) $\beta = -4$ (this can be validated by (23) and (8)) and 2) $\phi_C = V_{gs} - V_{th}$ (this can be obtained by letting $\phi_C = 0$ in (8) to develop the classical long-channel threshold voltage for JLCNFET). Note that in Ref. [20], the classical electron density of $Q_{m,cla} = -n_i R^2 \pi V_T \exp[(V_{gs}-V_{th})/V_T]$ for JBCNFET is essentially different from (25c) due to their different operational mechanisms. JLCNFET is for depletion-typed operation and JBCNFET is for inversion-typed operation. The electron charge density of $Q_{m,cla}$ in JBCNFET is linearly proportional to the silicon film diameter in contrast with the electron charge density of $Q_{m,cla}$ in JLCNFET that is linearly proportional to the subthreshold current factor β. According to (24) and with the criterion of $V_{gs} < V_{th} + \Phi_{QM}$, increasing the gate voltage can induce more Q_m, which hence brings about more subthreshold current. More details about the dependence of the subthreshold current on the gate voltage for different device parameters are demonstrated in the section 6.

5. SUBTHRESHOLD SWING DERIVATION

A) Short-channel case:

According to the definition of the subthreshold swing,

$$SS = [\frac{\partial \log I_{sub}}{\partial V_{gs}}]^{-1} \tag{26}$$

the subthreshold swing (SS) for short-channel JLCNFET can be obtained by substituting (21) into (26). It leads to

$$SS = \ln 10 \times \left[\frac{\exp(\frac{\Phi_{S,\min}}{V_T})\frac{d\Phi_{S,\min}}{dV_{gs}} - \exp(\frac{\Phi_{C,\min}}{V_T})\frac{d\Phi_{C,\min}}{dV_{gs}}}{V_T(\exp(\frac{\Phi_{S,\min}}{V_T}) - \exp(\frac{\Phi_{C,\min}}{V_T}))} - \left(\frac{\beta C_{ox}}{qN_d t_{si}}\right)\left(1 - \frac{\partial \Phi_{S,\min}}{\partial V_{gs}}\right) \right]^{-1} \tag{27}$$

Being similar to (22a), the central potential is larger than the surface potential for JLCNFET, which results in $\exp(\frac{\Phi_{C,\min}}{V_T}) >> \exp(\frac{\Phi_{S,\min}}{V_T})$. Therefore, (27) can be further reduced to

$$SS = \ln 10 \times \left[\frac{1}{V_T}\left(\frac{\partial \Phi_{C,\min}}{\partial V_{gs}}\right) - \left(\frac{\beta C_{ox}}{qN_d t_{si}}\right)\left(1 - \frac{\partial \Phi_{S,\min}}{\partial V_{gs}}\right) \right]^{-1} \tag{28}$$

with

$$\begin{cases} \dfrac{d\Phi_{C,\min}}{dV_{gs}} = 1 + \dfrac{ab^{'} + ba^{'}}{\sqrt{ab}} \\ \dfrac{d\Phi_{S,\min}}{dV_{gs}} = \dfrac{4C_{si}}{4C_{si} + C_{ox}} \dfrac{d\Phi_{C,\min}}{dV_{gs}} + \dfrac{C_{ox}}{4C_{si} + C_{ox}} \end{cases} \tag{29}$$

where

$$\begin{cases} a^{'} = \dfrac{e^{-L/\lambda_C} - 1}{2\sinh(L/\lambda_C)} \\ b^{'} = \dfrac{1 - e^{L/\lambda_C}}{2\sinh(L/\lambda_C)} \end{cases} \tag{30}$$

By substituting (29) and (30) into (28), the subthreshold swing for short-channel JLCNFET can be achieved.

B) Long-channel case:

For a long-channel JLCNFET, the coefficients of a and a' in (10) and (30) will approach zeros (i.e., $a = a^{'} \approx 0$ in (10) and (30)). Both the minimum surface and minimum central potentials and their derivatives with respect to gate voltage will be given by $\Phi_{S,\min} = \phi_S$, $\Phi_{C,\min} = \phi_C$, $\frac{d\Phi_{C,\min}}{dV_{gs}} = 1$, and $\frac{d\Phi_{S,\min}}{dV_{gs}} = 1$. Therefore, the subthreshold swing in (28) can be readily found as

$$SS = \ln 10 \times \left[\frac{1}{V_T} \left(\frac{\partial \Phi_{C,\min}}{\partial V_{gs}} \right) - \left(\frac{\beta C_{ox}}{qN_d t_{si}} \right) \left(1 - \frac{\partial \Phi_{S,\min}}{\partial V_{gs}} \right) \right]^{-1} \approx \ln 10 \times \left[\frac{1}{V_T} \right]^{-1} \quad (31)$$

It should be pointed that subthreshold swing of (31) is around 60mV/dec that is the ideal subthreshold swing for long-channel JLCNFETs [21]-[23].

6. Results and Discussion

The three-dimensional device simulator "*DESSIS*" [24] is used to validate the proposed model. For simplicity, the source/drain regions are assumed zero thicknesses in deriving the analytical model. Fig.2 demonstrates how the electron density is influenced by the gate voltage for both classical and quantum cases. It can be seen that the electron density for quantum case is smaller than that for classical case due to QMEs that equivalently increase the channel potential barrier, which hence increases the threshold voltage and decreases the electron charge density. Furthermore, the silicon film of t_{si}=2 nm results in strong QMEs and reduces more electron density than the other two silicon films of t_{si}=5 nm and 10 nm. Fig.3 plots the subthreshold current factor of β versus the channel length for different gate voltages. When the channel length is greater than 50 nm, the factor of β will approach -4 for the long-channel device. As L is smaller than 50 nm, |β| will be increased by SCEs together with the small gate voltage. This implies that SCEs together with a small gate voltage will increase |β| and brings about the large subthreshold current. Fig.4 shows the dependence of subthreshold current on the gate voltage for different silicon film diameters. The decreased silicon film diameter can result in the small subthreshold leakage current by reflecting the effects of thin silicon body on weak SCEs and strong QMEs. Being similar to SCEs, QMEs will decrease the subthreshold leakage current when the silicon film diameter is decreased. The plot indicates that to efficiently reduce the subthreshold leakage current, the small silicon diameter of t_{si}=5 nm is more desirable than t_{si}=10 nm, 15 nm. To investigate how the gate oxide thickness affects the subthreshold current, Fig.5 shows the dependence of the subthreshold current on the gate voltage with the gate oxide thickness as a parameter. The thinnest gate oxide of t_{ox}=1 nm will suffer the least SCEs and brings about the smallest subthreshold leakage current among the three gate oxide thicknesses of t_{ox}=1 nm, 2 nm, and 3 nm. In spite of reducing the subthreshold leakage current, a thin gate oxide can induce the gate leakage current due to the quantum tunneling effects [25]. How to reduce the subthreshold current without increasing the gate leakage current must be considered in designing the device with a thin gate oxide. Fig.6 plots the subthreshold current versus the gate bias for different workfunctions. The smallest workfunction of 4.1eV will cause the largest subthreshold leakage current among the three workfunctions of 4.1eV, 4.6eV, and 5.1eV. Although a small workfunction of 4.1eV can result in large subthreshold current, it will induce a small flat-band voltage that is very essential for the low operating power (LOP) circuits. The trade-off about how to take advantage of the low standby power (LSTP) operation without increasing the subthreshold leakage current must be taken into account as a small gate workfunction is applied for the device. Fig.7 shows the dependence of the subthreshold current on the gate bias for different silicon doping densities. The silicon film

with the large doping density of $N_d=3\times10^{19}\text{cm}^{-3}$ will cause more subthreshold leakage current than the other two small doping densities of $N_d=2\times10^{19}\text{cm}^{-3}$ and $N_d=1\times10^{19}\text{cm}^{-3}$. Fig. 8 shows the variation of subthreshold swing with the channel length for different silicon film diameters. As the channel length is decreased, the silicon film with a small diameter of t_{si}=5 nm can effectively decrease the subthreshold swing. On the contrary, the silicon body with t_{si}=10 nm and 15 nm can result in the large subthreshold swing and increase the static power consumption. The effect of the gate oxide thickness on the subthreshold swing is demonstrated in Fig.9. As the channel length is decreased, SCEs like DIBL will be enhanced, which hence gives rise to the large subthreshold swing. Among the three gate oxide thicknesses of t_{ox}=1 nm, 2 nm, and 3 nm, the smallest one of t_{ox}=1 nm shows the best immunity to SCEs and reduces the subthreshold swing most efficiently. Fig.10 depicts the dependence of the subthreshold swing on the channel length for different drain voltages. As L is reduced, the large drain voltage can bring about severe DIBL and increases the subthreshold swing. The low drain bias is preferred to suppress the subthreshold swing degradation. For FETs, the subthreshold swing of the short-channel device should not exceed 10%~15% subthreshold swing of the long-channel device. (i.e., $SS \le 70mV/dec$) to ensure the low-power operation [26].Therefore, with a criterion of the maximum allowed subthreshold swing (i.e., $SS = 70mV/dec$) for JLCNFET, the designing space for both the silicon film diameter and gate oxide thickness can be illustrated in Fig.11. For the channel length of L=30 nm, the required designing space can be much larger than that for the channel lengths of L=20 nm and L=15 nm. For instance, at t_{ox}= 3nm, L=30 nm can provide the silicon film thickness of t_{is}=12.5 nm that is larger than the silicon thicknesses of t_{si}=7.5 nm and t_{si}=5 nm provided by L=20 nm and L=10 nm, respectively. The comparison of the subthreshold swing between JLCNFET and JLDGFET is demonstrated in Fig.12. Note that the subthreshold swing model for the short-channel JLDGFET can be developed by following the same procedures shown in this paper. Fig.12 shows that JLCNFET is superior to JLDGFET in reducing the subthreshold swing due to the fact that JLCNFET has the better gate control over the channel and suppresses the SCEs more efficiently than JLDGFET. Besides SCEs and QMEs, BTBT effects may arise when the heavily doped JLCNFET, which is fully depleted in the OFF state, results in a significant band overlap between the channel and drain region. This band overlap leads to a BTBT of electrons from the channel to the drain in n-channel JLCNFETs. Tunneling current is observed to be a strong function of the silicon body thickness. BTBT will increase the subthreshold current especially for the device with a thick silicon film that significantly reduces the tunneling width between the conduction band of the channel and valence band of the drain [27]. To account for how BTBT effects impact the subthreshold current for the n-channel JLCNFET, we need to solve for the electron transmission coefficient (ETC) from the valence band of the channel to the conduction band of the drain. ETC will be substituted into the Fermi-Dirac function difference between the valence band and conduction band to find the net current flux [28]. However; this issue goes beyond the scope of the study and will not be addressed in this paper.

7. CONCLUSION

An analytical subthreshold current/swing model for JLCNFETs is developed based on the PPA, the DDA with effective BGW, and the scaling theory. In addition to SCEs, QMEs are included by accounting for effective BGW in deriving the model. The model explicitly demonstrates how the bulk doping density, oxide thickness, gate workfunction, drain bias, channel length, and silicon film diameter take an effect on the subthreshold current/swing. The model not only offers a physical insight into the device physics but also provides the basic designing guidance for JLCNFET. With appropriate modification, the model can also be extendable to JLDGFET.

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