

A COMPARATIVE STUDY OF TWO SECOND-ORDER SWITCHED-CAPACITOR BALANCED ALL-PASS NETWORKS WITH DIFFERENT INTEGRATORS

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Abstract: A recently proposed gain- and offset- compensated (GOC) fully differential switched-capacitor (SC) integrator is presented. The resulting gain, phase and offset errors are simultaneously lower when compared to the uncompensated balanced Hsieh-81 integrator. Both the integrators are used as building blocks of two SC second-order balanced all-pass networks. To demonstrate the superiority of the new integrator the two all-pass topologies were designed for a given transfer function and then compared in terms of four performances comprising sensitivities to finite op. amp. gain and offset voltage, capacitance spread and total capacitance. The component counts are also compared.

Key words: Filters, gain compensation, offset compensation, operational amplifiers, switched-capacitor integrators.

1. Introduction

The most important frequency limitation in switched-capacitor (SC) circuits is imposed by the operational amplifier (op. amp.) gain-bandwidth restrictions. A finite bandwidth GB reduces the speed of the op. amp. by introducing a limit on the sampling frequency $f_S = 1/T_S$ in order to assure a full charge transfer during the individual clock phase. But, in SC circuits the distortion introduced by the finite gain A_0 is more pronounced than that of the finite bandwidth [1]. On the other hand, an optimum trade-off between speed and gain is a critical design aspect because they are contradictory requirements. Generally, the price to be paid for high speed is low dc gain

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A_0 . The input-referred op. amp. offset voltage V_{os} introduces an output offset voltage which may become a significant limitation to the permissible signal swing. With the implementation of gain- and offset- compensation (GOC) technique the effect due to A_0 and V_{os} can be reduced.

It is well known that single-ended SC circuits have a very poor power supply rejection ratio (PSRR). Figures range from 20 to 40 dB [2], [3]. SC filtering techniques have been widely applied to voice-band applications requiring dynamic range on the order of 85 dB [3]. The use of balanced, i.e., fully differential structures for the realization of SC networks has many advantages. The fully differential topology is a powerful designing tool for improving the dynamic range and PSRR characteristics of SC filters [4]. The clock feedthrough noise is also reduced [5]. The fully differential solution offers a sign inversion at no extra cost, by simply crossing the signal lines. In this way higher-order structures without any extra element (e.g. inverting stages) can be built. Two disadvantages to the balanced technique are that the interconnection problem makes circuit layout more complex, and that a differential to single-ended conversion may be necessary in some applications. The basic building block of many balanced structures is the fully differential SC integrator, proposed by Hsieh et al (Fig. 7 of [3]). This integrator is a balanced version of the single-ended non-GOC basic-79 integrator (Fig. 1(a) of [6]). According to [6], for each integrator the name of the first author is assigned to the circuit, along with the year of publication. The inverting and noninverting Hsieh-81 integrators have been used as building blocks of balanced low-pass biquads [7],[8] and all-pass filters [9], [10]. A balanced version of the single-ended GOC Shafeeu- 91 integrator (Fig. 1 of [11]) was proposed in [12]. The resulting gain, phase and offset errors are considerably smaller than those of the non-GOC Hsieh-81 integrator.

In this paper two SC second-order balanced all-pass networks are considered. Subsequently, the Hsieh-81 integrators in the original structures have been replaced by the fully differential inverting GOC integrator, proposed in [12], and its noninverting counterpart. To demonstrate the superiority of this integrator the two all-pass topologies were designed for a given transfer function and then compared in terms of four performances comprising sensitivities to finite op. amp. gain and offset voltage, capacitance spread and total capacitance. The component counts are also compared.

2. Fully Differential Gain- and Offset- Compensated SC Integrator

The proposed in [12] fully differential modification of the single-ended

GOC inverting Shafeeu-91 integrator [11] is shown in Fig. 1(a), where $C'_1 = C''_1 = C_1$, $C'_2 = C''_2 = C_2$, $C'_h = C''_h = C_h$, $k = C_1/C_2$, and $k' = C_h/C_2$.

Compared with the non-GOC Hsiech-81 integrator the op. amp. has been replaced with the block shown in Fig. 1(a). In addition to the clock phases 1 and 2, the integrator requires two nonoverlapping clocks, e and o , shown in Fig. 1(b). The output voltage is sampled in phase $1o = 1 + o$. The value of the holding capacitors $C'_h = C''_h = C_h$ is not critical and can be made very small. In most applications it will be adequate to set C_h equal to the unit capacitance.

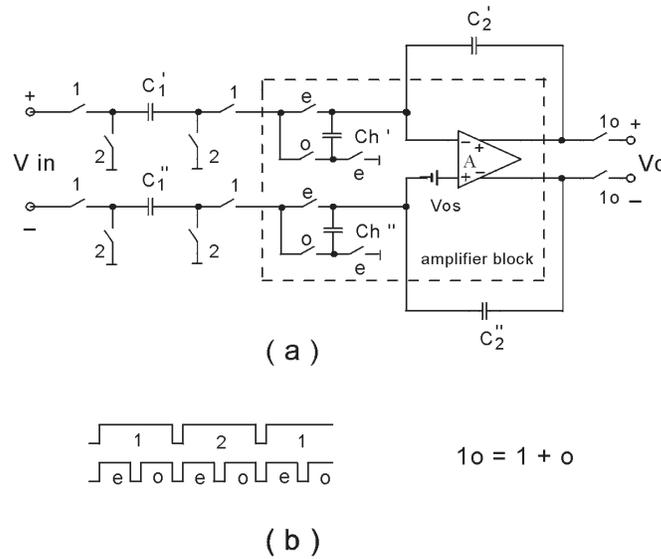


Fig. 1. Fully differential gain- and offset- compensated SC integrator.
 (a) Circuit architecture.
 (b) Clocking scheme.

The approximate formulas for the gain errors $m(\omega)$ and the phase errors $\theta(\omega)$ of the two integrators are given in Table 1. In both single-ended and fully differential cases (basic-79 integrator and Hsiech-81 integrator, correspondingly Shafeeu-91 integrator and novel integrator in Fig. 1) the expressions for $m(\omega)$ and $\theta(\omega)$ are identical. However, the error formulae for the integrator in Fig. 1 (Table 1) are more accurate than those given in [11] for the Shafeeu-91 integrator. The factor by which the phase error and the offset voltage error for the integrator from Fig. 1 are reduced, when compared to the Hsiech-81 integrator, is approximately given by $1/[(1+k)\mu]$. The gain

Table 1. Error formulas for SC integrators with finite op. amp. gain $A_o = 1/\mu$.

Integrator	Gain error $m(\omega)$	Phase error $\theta(\omega)$
Hsieich-81	$-(1 + \frac{k}{2})\mu - \frac{k^2\mu^2}{8 \tan^2(0.5\omega T_S)}$	$\frac{k\mu}{2 \tan(0.5\omega T_S)}$
in Fig. 1	$-k'\mu - \frac{[(1+k)(2+k) - 2k'(1+k+k')]\mu^2}{2}$	$\frac{k(1+k)\mu^2}{2 \tan(0.5\omega T_S)}$

error of the proposed integrator is reduced by at least a factor $1/k'$ ($k' < 1$).

3. Two All-pass Filter Topologies with Different SC Integrators

To compare the performances of the two all-pass topologies they were used to realize a particular discrete second-order all-pass transfer function with the following parameters: $f_o = f_P = 6400$ Hz, $Q_o = Q_P = 3$, and a sampling frequency $f_S = 128$ kHz.

The z -domain transfer function of this all-pass filter is

$$H(z) = \frac{z^{-2} - 1.8076406z^{-1} + 0.9005767}{1 - 1.8076406z^{-1} + 0.9005767z^{-2}} \quad (1)$$

3.1 SC all-pass biquad topology with different integrators

The balanced all-pass biquad from Fig. 2 of [9] is considered. Subsequently, the Hsieich-81 integrators in the original structure have been replaced by the inverting integrator from Fig. 1 and its noninverting counterpart. The circuit schema of the resulting filter is shown in Fig. 2. The capacitor values are $A=1.0698$, $B=3.3928$, $C=1$, $D=3.3928$, $E=1.0698$, $G=1$, $L=1.0698$, $K=3.0555$, $C_h=1$. As a customary, the capacitors were scaled so that the minimum capacitance incident on each op. amp. summing junction is 1.00 unit.

The ideal z -domain transfer function has the form

$$H(z) = \frac{K}{B} \frac{1 - \left[2 + \frac{A(L-G)}{DK}\right]z^{-1} + \left(1 + \frac{AL}{DK}\right)z^{-2}}{1 - \left[2 - \frac{A(C+E)}{BD}\right]z^{-1} + \left(1 - \frac{AE}{BD}\right)z^{-2}} \quad (2)$$

The same transfer function can be obtained in an unbalanced structure by connecting the L capacitor to negative of the input voltage. Normally, this

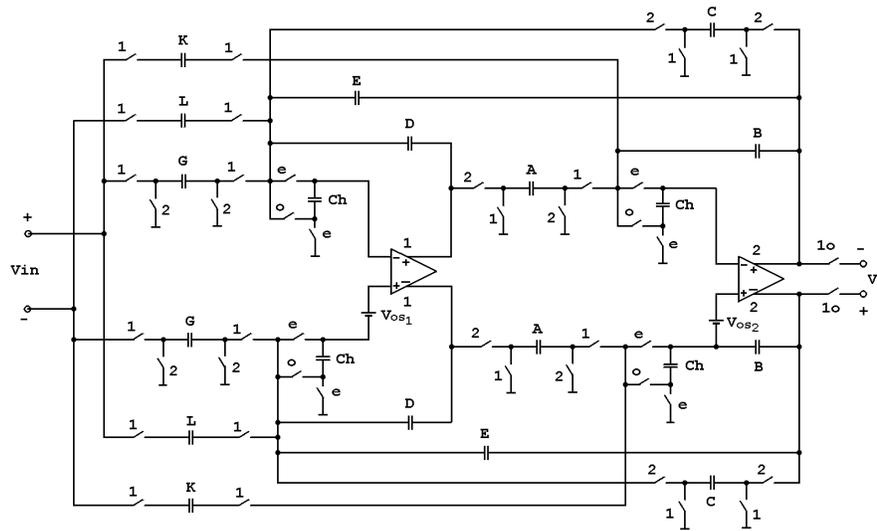


Fig. 2. Balanced all-pass biquad with GOC integrators.

will require an extra inverter stage. Since in a balanced regime both polarity inputs are available, the transfer function (2) is readily realized by merely cross-connecting two L capacitors. We shall assume that corresponding pairs of capacitors track each other exactly, so that the circuit is described exactly by (2).

Fig. 3 shows the deviations from the nominally flat amplitude response of the all-pass biquad designed with the Hsiech-81 integrator and with the GOC integrator in Fig. 1 for $A_0 = 100$.

It is obvious that the response of the circuit with the GOC integrator from Fig. 1 follows much more closely the ideal response than those of the design with the Hsiech-81 integrator.

The steady state output voltages of the all-pass biquad designed with the Hsiech-81 integrator and with the integrator from Fig. 1 for $A_0 = 100$, are respectively

$$\begin{aligned} \lim_{n \rightarrow \infty} V_o(n) &= 1.9967V_{os1} + 0.01997V_{os2} \\ \lim_{n \rightarrow \infty} V_o(n) &= 0.03414V_{os1} + 0.00420V_{os2} \end{aligned} \quad (3)$$

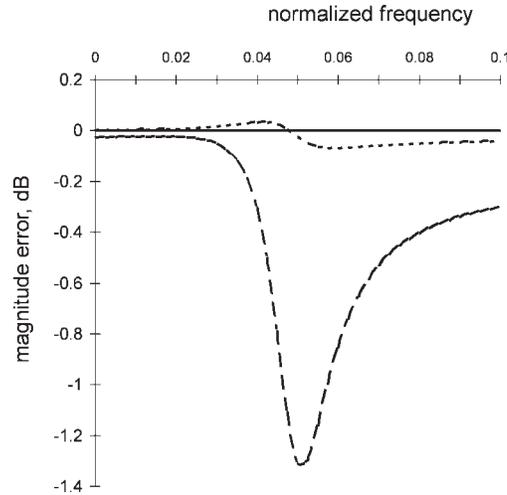


Fig. 3. Effect of finite op. amp. dc gain A_0 on the magnitude responses of the all-pass biquad topology:
 — ideal response ($A_0 \rightarrow \infty$),
 - - - with Hsiech-81 integrator ($A_0 = 100$),
 . . . with GOC integrator in Fig. 1 ($A_0 = 100$.)

3.2 SC all-pass ladder topology with different integrators

In [10], a new approach was presented for the exact discrete-time z -domain design and synthesis of SC LDI ladder all-pass network having general n -th order transfer function on the form

$$H(z) = \frac{z^n D(z^{-1})}{D(z)} \quad (4)$$

where $D(z)$ represents an n -th order strictly Hurwitz polynomial with real coefficients. The corresponding structure (employing a leapfrog configuration) requires $n+1$ op. amps. for its implementation, i.e. only one op. amp. more than the theoretical minimum under a two-phase clocking scheme. The SC implementation has been obtained by employing inverting and non-inverting Hsiech-81 integrators.

A second-order SC LDI ladder all-pass filter is shown in Fig. 4 where the Hsiech-81 integrators have been replaced by the inverting integrator from Fig. 1 and its noninverting counterpart.

The required clock waveforms are depicted in Fig. 1(b). The subcircuit associated with the topmost op. amp. 1 acts as SC adder for producing

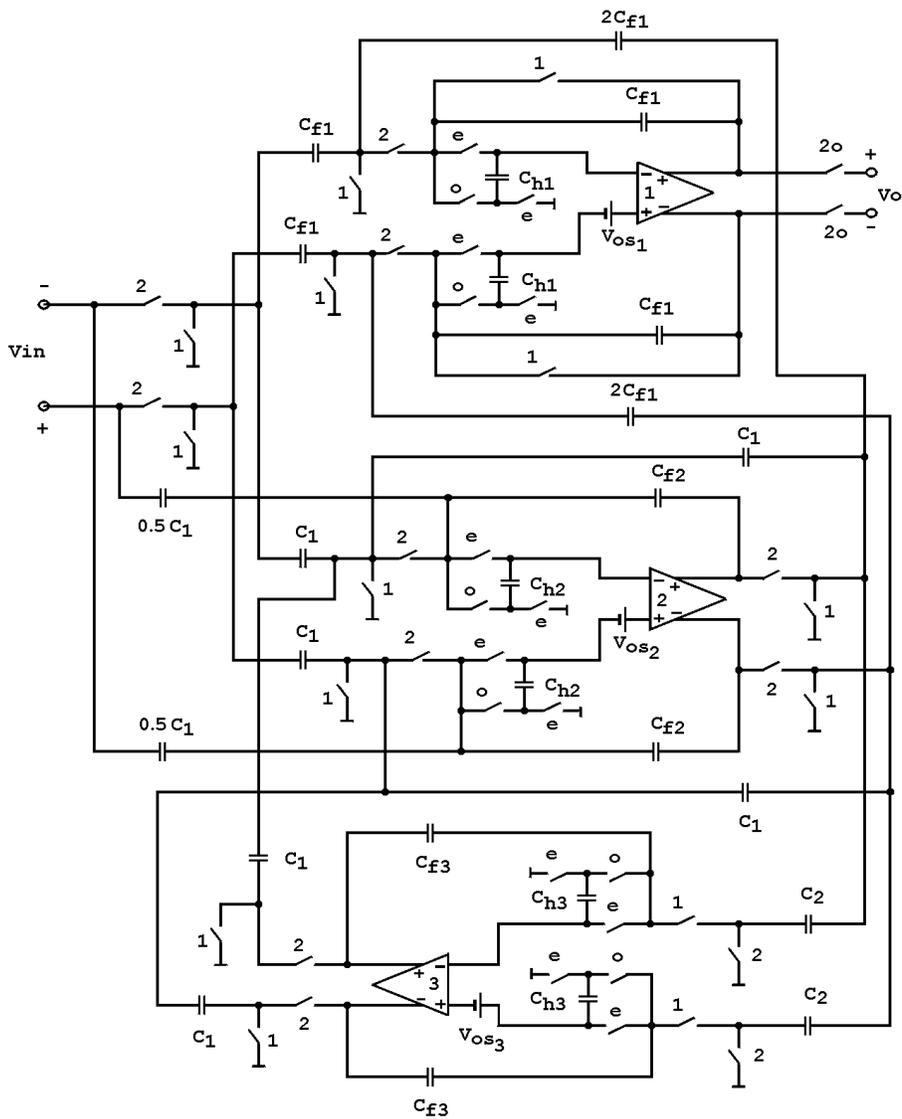


Fig. 4. Balanced ladder all-pass filter with GOC integrators.

the transfer function $H(z)$ as a combination of its constituent decomposed parts. However, during the intervals 1 the output voltage of op. amp. 1 is pulled near to zero (V_{os1}), and the op. amp. must have a high slew rate and

fast settling time to enable the output to slew back and forth at each clock transition.

The normalized capacitor values are $C_1 = 2$, $C_2 = 1$, $C_{f1} = 1$, $C_{f2} = 18.1160$, $C_{f3} = 1.0698$, $C_{h1} = C_{h2} = C_{h3} = 1$.

The ideal z -domain transfer function has the form

$$H(z) = \frac{1 - \left[2 + \frac{C_1}{C_{f2}} \left(1 - \frac{C_2}{C_{f3}}\right)\right] z^{-1} + \left(1 + \frac{C_1}{C_{f2}}\right) z^{-2}}{1 + \frac{C_1}{C_{f2}} - \left[2 + \frac{C_1}{C_{f2}} \left(1 - \frac{C_2}{C_{f3}}\right)\right] z^{-1} + z^{-2}} \quad (5)$$

Fig. 5 shows the deviations from the nominally flat amplitude response of the ladder all-pass filter designed with the Hsiech-81 integrator and with the GOC integrator in Fig. 1 for $A_0 = 100$.

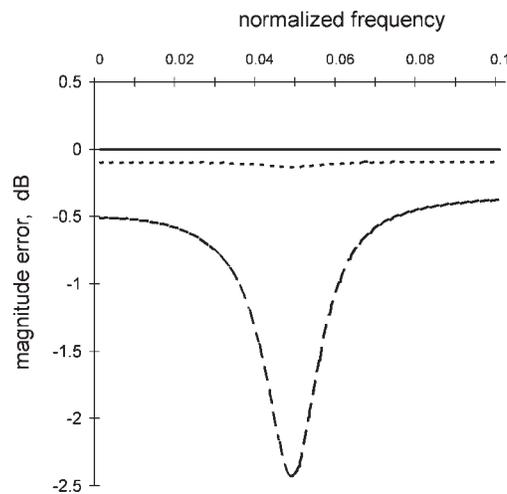


Fig. 5. Effect of finite op. amp. dc gain A_0 on the magnitude responses of the ladder all-pass topology:
 — ideal response ($A_0 \rightarrow \infty$),
 - - - with Hsiech-81 integrator ($A_0 = 100$),
 . . . with GOC integrator in Fig. 1 ($A_0 = 100$).

It is obvious that the response of the circuit with the GOC integrator from Fig. 1 follows much more closely the ideal response than those of the design with the Hsiech-81 integrator. The steady state output voltage of the all-pass biquad designed with the Hsiech-81 integrator and with the

integrator from Fig. 1 for $A_0 = 100$, are, respectively

$$\begin{aligned} \lim_{n \rightarrow \infty} V_o(n) &= 3.84615V_{os1} - 0.05710V_{os2} + 1.90374V_{os3} \\ \lim_{n \rightarrow \infty} V_o(n) &= 0.11968V_{os1} - 0.06695V_{os2} + 0.04295V_{os3} \end{aligned} \tag{6}$$

3.3. Comparison of the two all-pass topology

Fig. 6 shows the deviations from the nominally flat amplitude response due to op. amp. finite gain $A_0 = 100$ for the two all-pass topologies designed with the GOC integrator from Fig. 1.

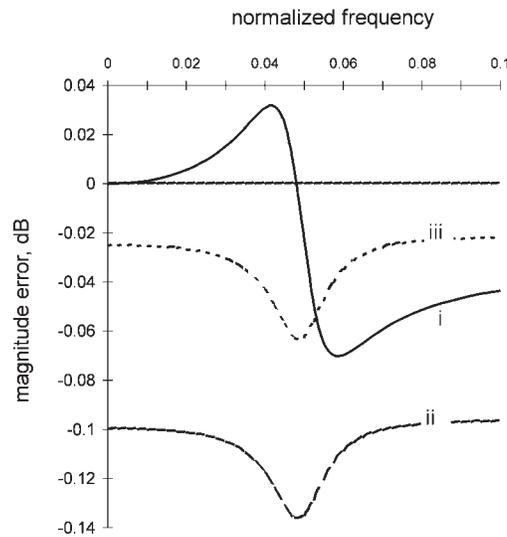


Fig. 6. Magnitude responses of the two all-pass GOC topologies: case i) all-pass biquad topology from Fig. 2, case ii) all-pass ladder topology from Fig. 4 ($C_2 = 1, C_{f1} = 1, C_{f3} = 1.0698$), case iii) all-pass ladder topology from Fig. 4 ($C_2 = 10, C_{f1} = 10, C_{f3} = 10.698$).

Compared the two all-pass designs we note that the error in case ii) is about twice worse than case i). To reduce the influence of the finite op. amp. gain on the magnitude response of the all-pass ladder topology from Fig. 4 the capacitance ratios $k'_1 = C_{h1}/C_{f1}$ and $k'_3 = C_{h3}/C_{f3}$ must be smaller. The corresponding curve, (case iii), for $k'_1 = 0.1$ ($C_{f1} = 10$) and $k'_3 = 0.09348$ ($C_{f3} = 10.698, C_2 = 10$) is depicted in Fig. 6. In this case the two all-pass topologies have nearly the same maximum magnitude errors,

but the total capacitance of the ladder topology is approximately five time larger.

Table 2 compares the complexities of the two all-pass topologies in terms of component count and area requirement.

Table 2. Comparison of the complexity of the two all-pass topologies

Circuit	number op. amps.	number C	number switches	total C	C spread
biquad topology	2	18	46	34.101	3.393
ladder topology ($C_2 = 1$, $C_{f1} = 1$, $C_{f3} = 1.0698$)	3	26	46	68.3761	18.116
ladder topology ($C_2 = 10$, $C_{f1} = 10$, $C_{f3} = 10.698$)	3	26	46	177.628	18.116

4. Conclusion

A recently proposed balanced version of the single-ended gain- and offset- compensated Shafeeu-91 integrator have been compared with the earlier one uncompensated Hsiech-81 integrator. The errors of the novel integrator are considerably smaller. The feasibility of this integrator has been demonstrated by designing two SC balanced all-pass topologies for a given second-order transfer function. The resulting networks have better performances than the same circuits based on the Hsiech-81 integrator.

The all-pass biquad topology with GOC integrators has a maximum capacitor ratio of 3.393 and a total capacitance of 34 units. This is a significant saving over the SC all-pass ladder topology with GOC integrators, which needed 178 units of capacitance and a capacitance spread of 18.116 for the same maximum magnitude error.

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