FACTA UNIVERSITATIS
Ser: **Elec. Energ.** Vol. 25, N^{o} 2, August 2012, pp. 161 - 170
DOI: 10.2298/FUEE1202161A

LINEARIZATION OF SYMMETRICAL AND ASYMMETRICAL TWO-WAY DOHERTY AMPLIFIER

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Abstract. *The linearization effects on two-way Doherty amplifiers are presented in this paper. Symmetrical Doherty amplifier with the additional circuit for linearization has been realized and measurements of the linearization influence on the third- and fifth-order intermodulation products have been carried out. Asymmetrical Doherty amplifier has been designed and effects of the applied linearization technique have been considered through the simulation process. The linearization approach uses the fundamental signals' second harmonics and fourth-order nonlinear signals that are extracted at the output of the peaking cell, adjusted in amplitude and phase and injected at the input and output of the carrier cell in Doherty amplifier.*

Key words: *Doherty amplifier, linearization, second harmonics and fourth-order nonlinear signals, intermodulation products*

1. INTRODUCTION

With the advent of spectrally efficient wireless communication systems, the linearization techniques for nonlinear microwave power amplifiers have gained significant interest. Demanding requirements of new systems (CDMA2000, W-CDMA, OFDM etc.), to meet both linearity and high power efficiency present a serious task for transmitter designers. The Doherty amplifier is capable of achieving high efficiency of power amplifiers in base station. Different linearization methods of Doherty amplifier for reducing nonlinear distortions while keeping the power amplifier in the efficient mode have been reported: post-distortion-compensation [1], the feedforward linearization technique [2], the predistortion linearization technique [3] and combination of those two linearization techniques [4].

The linearization effects of the fundamental signals' second harmonics (IM2) and fourth-order nonlinear signals (IM4) at frequencies that are close to the second harmonics to the standard (two-way, three-way and three-stage) Doherty amplifiers were investigated in [5] and [6] through the simulation process. We applied the approach where IM2 and IM4 signals are injected together with the fundamental signals into the carrier amplifier

Received November 19, 2012
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* **Acknowledgement**: This work was supported by the Ministry of Education and Science of Republic of Serbia, the project number TR-32052.

input and put at its output [7]. Additionally, the influence of IM2 and IM4 signals on Doherty amplifier linearity was verified experimentally on standard two-way Doherty amplifier in two cases: when linearization signals are led to the input of carrier cell [8] and when they are injected at the output of carrier cell [9].

This paper presents experimental verification of the linearization approach on realized symmetrical two-way Doherty amplifier with the additional circuit for linearization. Also, an asymmetrical two-way Doherty amplifier has been designed and linearization results are considered through the simulation process. The linearization technique utilizes the second harmonics and fourth-order nonlinear signals at frequencies close to the second harmonics which are generated at the output of the peaking cell. The signals for linearization are tuned in amplitude and phase through the linearization branches and run at the carrier amplifier input and output over the frequency diplexers.

2. LINEARIZATION

Theoretical analysis of the linearization approach that uses the second harmonics (IM2) and fourth-order nonlinear signals (IM4) for linearization has been given in [5], and [7]. According to this, it is possible to reduce spectral re-growth caused by the third-order distortion of the fundamental signal by choosing the appropriate amplitude and phase of IM2 signals injected at the input and output of the amplifier. Additionally, the fifth-order intermodulation products can be suppressed by IM4 signals inserted at the amplifier input and output.

The IM2 and IM4 signals generated at the output of peaking amplifier are extracted through the frequency diplexer circuit in configuration depicted in [5]. It separates the fundamental signals and signals for linearization (IM2 and IM4 signals) that are matched to the impedance optimal for their adequate power level. The IM2 and IM4 signals are tuned in amplitude and phase by the amplifier and phase shifter over two independent linearization paths. They are inserted at the carrier amplifier input and output over the frequency diplexers designed with the independent matching circuits for the fundamental and signals for linearization. This configuration provides the linearization of Doherty amplifier by the simultaneous injection of IM2 and IM4 signals at the input and output of the carrier amplifier.

3. DESIGN OF AMPLIFIER AND LINEARIZATION CIRCUITS

Agilent Advanced Design System-ADS software has been used for the design of conventional two-way Doherty amplifier whose schematic diagram is shown in Fig. 1. An optional attenuator placed before the carrier cell in Doherty amplifier makes differences between the symmetrical (without attenuator) and asymmetrical (with attenuator) Doherty amplifier.

Two-way Doherty amplifier was designed in standard configuration [1], [2], [4], [5]. The frequency diplexer at the input and output of the carrier cell and at the output of the peaking cell filters the fundamental signals and signals for linearization at the frequencies around the second harmonics.

The input and output matching circuits of amplifying cells transform the input impedance of the device to 50Ω and the optimum load impedance Z_{OPT} to 50Ω, [10]. In the low-power region, the peaking amplifier should be an open circuit and load impedance of the carrier amplifier should be doubled to $2Z_{OPT}$ by a quarter-wave impedance transformer with the characteristic impedance $R_o = 50\Omega$. Also, quarter-wave transmission line with the characteristic impedance $R_t = R_o\sqrt{2}$ transforms 50Ω to 25Ω that is a load impedance of the output combining circuit when the peaking amplifier is turned on in a higher power region. Phase difference of 90° is required at the inputs of the carrier and peaking amplifiers to compensate for the same phase discrepancy between those two amplifiers caused by the quarter-wave impedance transformer at the output.

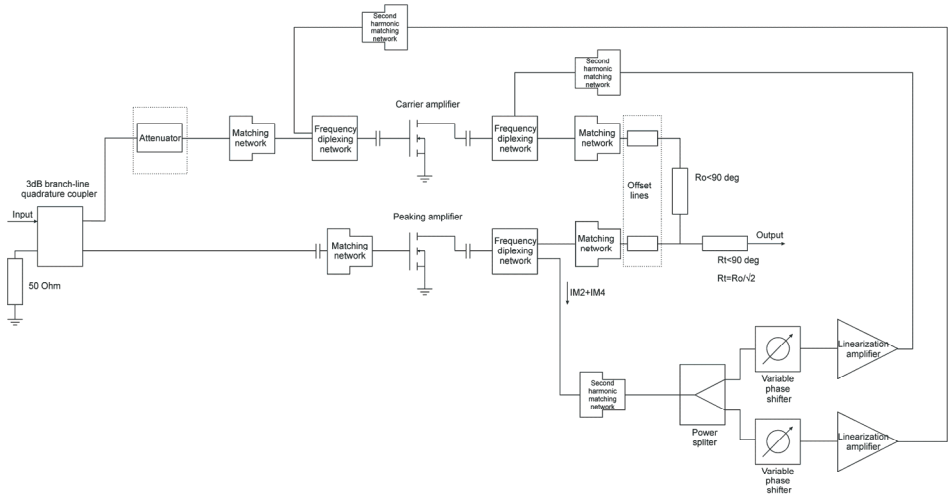


Fig. 1. Schematic diagram of two-way Doherty amplifier with additional circuit for linearization

The output impedance of the LDMOSFET is strongly reactive with a low resistance, so that, in a low-power region, considerable power leaks from the carrier amplifier to the peaking amplifier. The impedance seen at the output of the peaking transistor is transformed to the open by the output matching circuit and the proper offset line [10].

3.1. Symmetrical Doherty amplifier

The carrier and peaking cells in symmetrical Doherty amplifier (Fig. 2.) were designed using Freescale's MRF281S LDMOSFET which non-linear MET model is incorporated in ADS library. The transistor shows a 4W peak envelope power. The matching impedances for source and load at 1GHz are $Z_S = (5.5 + j15)\Omega$ and $Z_L = (12.5 + j27.5)\Omega$, respectively. These impedances were obtained by using load-pull and source-pull analysis in ADS. The matching impedances for the second harmonics at 2GHz for source and load are $Z_S = (3.1 - j2.4)\Omega$ and $Z_L = (12.5 + j9.2)\Omega$, respectively. These impedances are taken from the authorized Freescale catalogue.

The carrier amplifier is biased in class-AB ($V_D = 26$V, $V_G = 5.1$V (13.5%I_{DSS})), whereas the peaking amplifier operates in class-C ($V_D = 26$V, $V_G = 3.2$V).

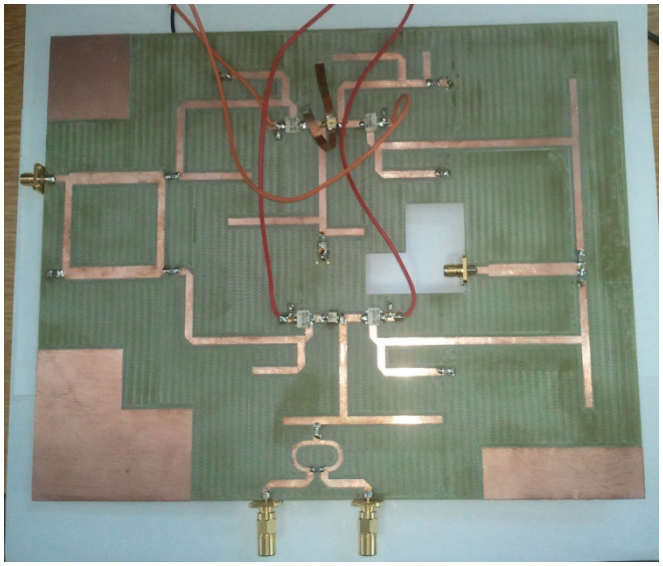


Fig. 2. Realized symmetrical two-way Doherty amplifier

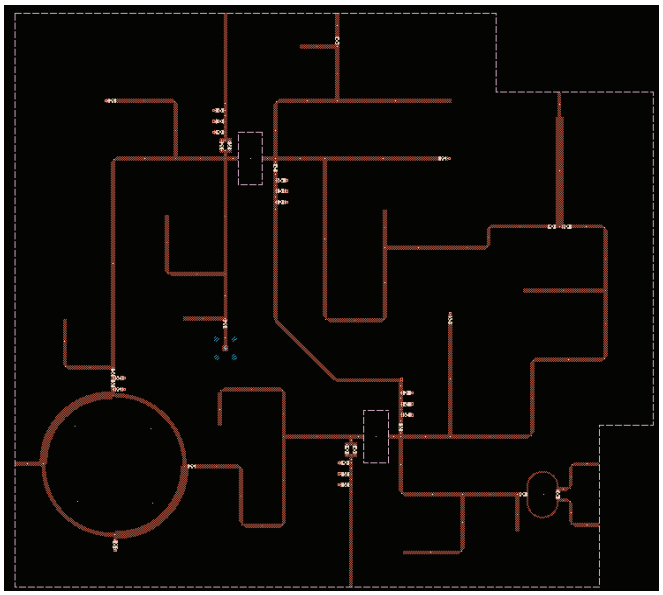


Fig. 3. Layout of asymmetrical two-way Doherty amplifier

3.2. Asymmetrical Doherty amplifier

The resistive Pi attenuator is placed before carrier cell to achieve asymmetry in amplifier design. In order to produce maximum power from both cells of Doherty amplifier and more linear operation, the peaking amplifier is driven by signal with 2dB higher power than that of the carrier amplifier according to the analysis of uneven power drive performed in [11]. Attenuator is projected as a matched attenuator with 2dB attenuation. Required exact values of the resistors are 11.61Ω for a serial resistor and 436.21Ω for shunt resistors. The resistors from the standard E24 resistor series closest to the desired ones, 12Ω for the serial resistor and 430Ω for the shunt resistors, are used to realize the attenuator that is characterized by VSWR=1.003 and attenuation of 2.06dB.

The carrier and peaking cells in asymmetrical Doherty amplifier (Fig. 3.) were designed by using AP602A-2 GaAs MESFET. The matching impedances for source and load at 0.9GHz for carrier cell are $Z_S = (17.5 + j90.1)\Omega$ and $Z_L = (53.1 + j28.8)\Omega$, respectively, whereas for the peaking cell they are $Z_S = (101.4 + j175.8)\Omega$ and $Z_L = (72.8 + j122.7)\Omega$. The matching impedances for the second harmonics at 1.8GHz for source and load are $Z_S = (15.0 + j44.8)\Omega$ and $Z_L = (48.1 + j30.2)\Omega$, respectively. All these impedances were obtained by using load-pull and source-pull analysis in ADS.

The carrier amplifier is biased in class-AB ($V_D = 5$V, $V_G = -4$V), and the peaking amplifier operates in class-C ($V_D = 5$V, $V_G = -6.8$V).

3.3. Linearization circuit

The linearization circuit (Fig. 4.) comprises M/A-COM PIN diode variable attenuator MA4VAT2007-1061T, two Mini-Circuits 180° voltage variable phase shifters JSPHS-23+ to provide phase shift of 360° and Skyworks high linear 2W power amplifier SKY65120. The linearization circuit adjusts IM2 and IM4 signals in amplitude and phase before they are inserted at the carrier amplifier input and output over the frequency diplexers. The linearization branch can vary power of the signals for linearization from -20dB to 10dB in reference to the generation point at the peaking amplifier output.

The symmetrical two-way Doherty amplifier and linearization circuit are realized on FR4 substrate with 1.55 mm thickness and 17.5μm metallization layer. The printed circuit boards for both circuits were manufactured on LPKF ProtoMat S100 in laboratory.

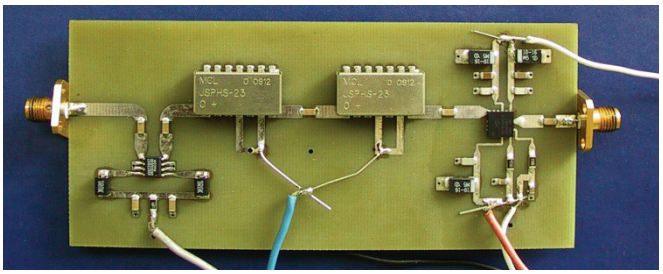


Fig. 4. Realized linearization circuit

The asymmetrical Doherty amplifier is designed on Rogers 3010 substrate with 1.6mm thickness and 17μm metallization layer.

With the intention of reducing the required number of laboratory DC power supplies, the separate integrated circuit, which includes ten independent DC bias outputs (Fig. 5), is realized by using standard voltage regulators. Five DC outputs are positive adjustable (from 0V to 15V), three are negative adjustable (from -1.2V to -8V) and two are fixed DC voltages (+12V and +5V). Required inputs are $+20V_{DC}$ and $-10V_{DC}$.

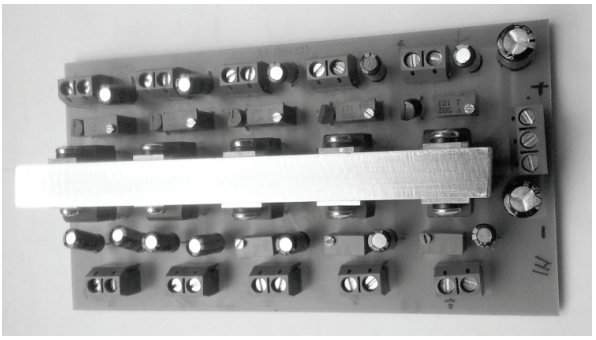


Fig. 5. Realized circuit for DC bias

4. RESULTS

S-parameters of the symmetrical Doherty amplifier obtained in simulation by ADS as well as measured parameters are shown in Fig. 6. The figure compares the characteristics achieved in case of simulated amplifier circuit with an ideal lossless substrate (dashed line) and in case when substrate losses are included into the analysis. One can notice that the amplifier operational frequency is slightly shifted from the designed.

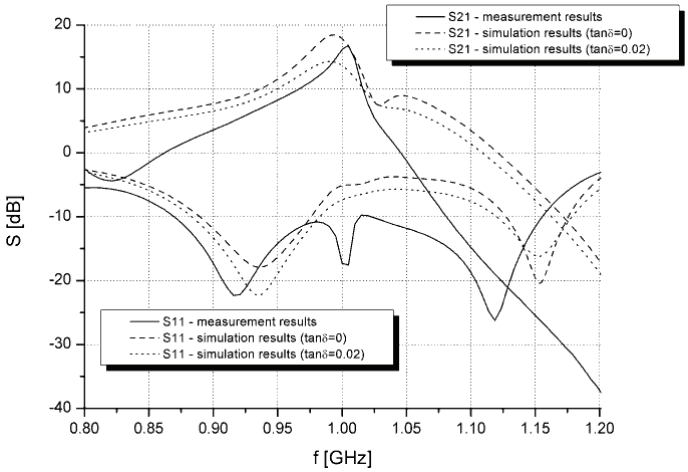


Fig. 6 S-parameters of symmetrical two-way Doherty amplifier

In order to experimentally verify the proposed linearization technique the standard two-tone test was applied at frequencies 1000MHz and 1001MHz. The results from Fig. 7 and Fig. 8 represent the simulated and measured results of the linearization of symmetrical two-way Doherty amplifier accomplished for the output power ranging from 16dBm to 25dBm. The upper signal power level is constrained by the laboratory equipment capability to the power that is 11dB below the maximal catalogue power level of the transistor engaged. These results are compared to the case when the linearization is not carried out. Fig. 7 relates to the power reduction of IM3 products at 999MHz (IM3-) and 1002MHz (IM3+), whereas Fig. 8 displays the results connected to the IM5 products at 998MHz (IM5-) and 1003MHz (IM5+). It follows from the figures that intermodulation products before linearization are at lower power levels when measurements are carried out than in simulation. The explanation for such behavior stems from different working conditions specified in simulation and occurring during measurements. Actually, simulation was performed for FR4 substrate characterized by some typical parameter values available in literature since they are not specified precisely by the manufacturers, and additionally, rise of working transistor temperature predicted in simulation differs in experimental conditions.

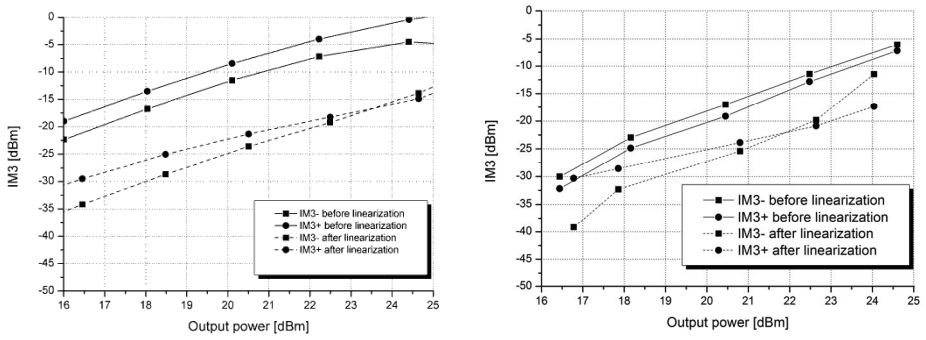


Fig. 7. Third-order intermodulation products before and after linearization of symmetrical two-way Doherty amplifier for a power range: a) simulated results; b) measured results

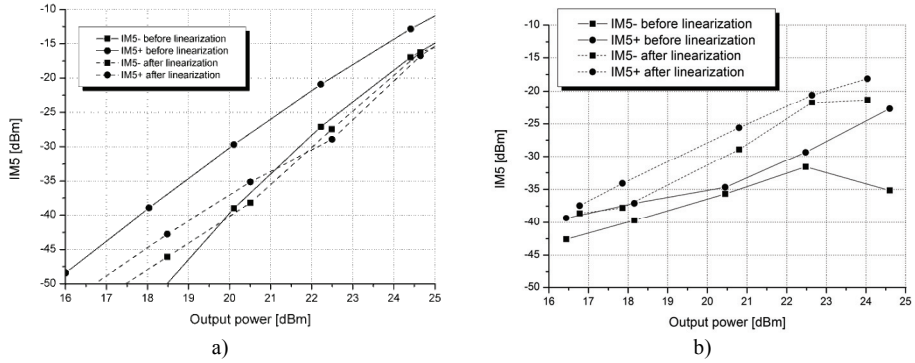


Fig. 8. Fifth-order intermodulation products before and after linearization of symmetrical two-way Doherty amplifier for a power range: a) simulated results; b) measured results

The results presented for the symmetrical Doherty amplifier relate to the case when the amplitudes and phases of IM2 and IM4 signals are fit to the optimal values for 22.5dBm output power. It is evident from these figures that the linearization with the proposed approach gives satisfactory results in the improvement of IM3 products for a range of output power. However, IM5 products increase slightly at the whole power range considered, though IM5 products are kept at the power level close to the linearized IM3 products. According to the theoretical analysis of the linearization approach ([5]), IM3 and IM5 products can be reduced simultaneously, in case when both amplitudes and phases of IM2 and IM4 signals are related properly. On the contrary, only one kind of the intermodulation products can be suppressed sufficiently whereas the other will not be lowered or even it can increase in power. This situation is more probable when only one source of IM2 and IM4 signals is exploited for linearization.

Drain efficiency (DE) obtained in simulation for the symmetrical two-way Doherty amplifier with the ideal lossless substrate is compared in Fig. 9 with the simulated characteristic attained for the circuit with the real FR4 substrate and measured one, all in case when the linearization is not applied. The good matching can be observed between curves relating to the simulated and experimental results up to 34dBm power. At this power level, there is a maximal difference between the simulated and measured result of 5%. The maximal efficiency achieved by the realized circuit is 32.7%.

When consumption of the circuit for linearization is included into analysis, DE decreases, so that, DE of linearized Doherty amplifier is lower than in case when linearization is not exploited, for example it is 7% lower at 25dBm total output power. The linearization branches for experimental application include the high gain amplifiers with significant DC consumption in addition to the variable attenuators to enable amplitude adjustment of the signals for linearization within a wide range. Consequently, DE is reduced more than it is expected in circuits for commercial application that comprise amplifiers with the expected lower gain and DC supply.

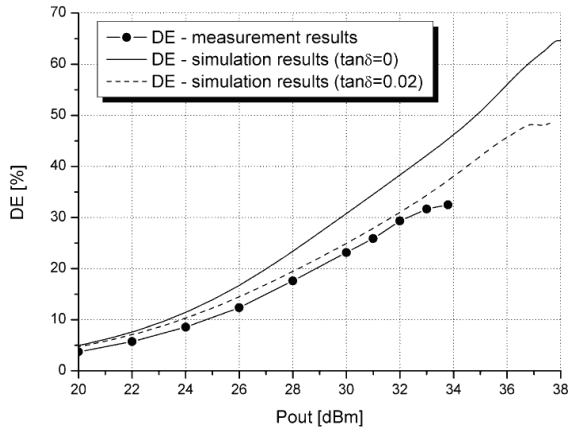
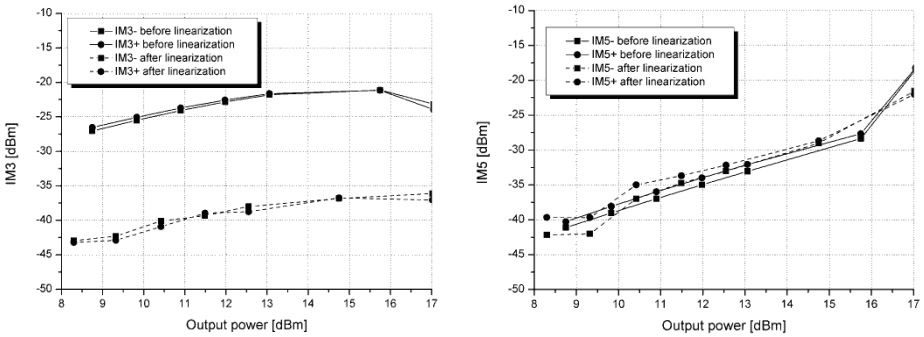


Fig. 9. Drain efficiency of symmetrical two-way Doherty amplifier

The effects of the applied linearization methods on the asymmetrical two-way Doherty amplifier have been considered through the simulation process by using two-tone test at

frequencies 899MHz and 901MHz. The obtained results are presented in Fig. 10 for the output power ranging from 8dBm to 17dBm that is 4dB below 1dB compression point. These results are compared to the case when linearization in not performed. Fig. 10a) refers to the power decrease of IM3 products at 897MHz (IM3-) and 903MHz (IM3+), whereas Fig. 10b) shows results associated with the IM5 products at 895MHz (IM5-) and 905MHz (IM5+). It is noticeable that the proposed linearization method achieves improvement of IM3 products of about 15dB in the power range, while IM5 products can be treated as almost unchanged. The process of asymmetrical Doherty amplifier fabrication is in progress.



a) b)

Fig. 10. Simulated intermodulation products before and after linearization of asymmetrical two-way Doherty amplifier for a power range: a) third-order; b) fifth-order products

5. CONCLUSION

This paper presents the verification of the linearization of two-way Doherty amplifier by the simultaneous injection of the second harmonics and fourth-order nonlinear signals (IM2 and IM4) at the input and output of the carrier amplifier. The linearization results for the symmetrical Doherty amplifier are experimentally confirmed. The analysis of linearization effects on asymmetrical Doherty amplifier is carried out through the simulation while the amplifier realization is in progress. The linearization approach provides a significant downtrend of the third-order intermodulation products, even for a wider power range, while the fifth-order intermodulation products rise slightly up to the acceptable level below the suppressed IM3 products.

It should be pointed out that the crucial matter in the approach used for Doherty amplifier linearization is the possibility to exploit the peaking amplifier as a source of the signals for linearization and therefore avoid the necessity for the additional nonlinear sources that will increase the circuit complexity and total energy consumption.

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