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INPUT-OUTPUT BASED QUASI-SLIDING MODE CONTROL OF DC-DC CONVERTER*

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Abstract. *The paper presents the design of discrete-time quasi-sliding mode voltage controller for DC-DC buck converter. The control algorithm is realized by measuring only sensed output voltage. No current measurements and time derivatives of output voltage are necessary. The proposed quasi-sliding mode controller provides stable output voltage, exhibiting robustness to parameter and load variations.*

Key words: *buck converter, discrete-time sliding mode, input-output measurements, minimum variance, PWM*

1. INTRODUCTION

Sliding mode control represents a class of particular interest in variable structure control systems [1], since it provides robust system motion along a predefined sliding surface. The most distinguished feature of the sliding mode control system is its insensitivity to parameter uncertainty and external disturbances under certain conditions [2], making this control strategy very suitable for power converting systems under load variation [3]. Theoretically, a sliding mode controller operates at infinitive, practically, at high and varying switching frequency, challenging its implementation in DC-DC converters due to switching, inductor and transformer core losses, as well as electromagnetic interference noise issues. These first sliding mode controllers for power converters were hysteresis-modulation based. In order to make sliding mode controller more applicable to DC-DC converters, its switching frequency should be limited, so it operates as an approximation of ideal sliding mode controller. This results in reduction of system robustness. The limitation is done by changing the modulation method from hysteresis-modulation to pulse width modulation (PWM), known as duty cycle control as well [4]. A unified approach to design of PWM based sliding mode voltage control of DC-DC buck, boost and buck-boost converters are presented in [5]. A nonlinear sliding mode controller design of DC-

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DC converter based on extended linearization technique is discussed in [6]. Fuzzy sliding mode control is proposed and also implemented in the design of DC-DC buck converter [7]. The control of two DC-DC buck converters connected in parallel, by using integral sliding mode control algorithms, is considered in [8].

The fixed switching frequency can also be achieved by using discrete-time sliding mode controllers. Discretization process of sliding mode control induces an undesirable chattering phenomenon in the vicinity of a sliding surface, causing the quasi-sliding motion [9] in that way. This means that the system trajectory is within some quasi-sliding area S comprising the sliding surface. The domain S possesses such invariant property which ensures that every system motion, which has arrived into S at some time instant $t_0 = K_0T$, remains in the domain for every $k > K_0$, k, $K_0 \in N$.

One approach to design of digital sliding mode like control of DC-DC buck converter is presented in [10]. In this paper, the combination of well-known minimum variance and discrete-time sliding mode control [11] and its implementation in the voltage control of DC-DC buck converter is considered. The result of such combination is the quasi-sliding mode control algorithm, based only on output voltage measurement, rejecting the need for the use of additional current sensors for control realization. Conventional current sensing methods, using a resistor as a sensor element, suffer from significant power losses, especially when the current is high. That is why the loss-less current sensing methods are used [12], whereas input-output control laws are more than preferable. The proposed quasi-sliding mode control approach also enables better system accuracy in steady state and provides chattering alleviation. This approach has already shown good results in control of AC voltage stabilizer [13].

The paper is organized as follows. In the second section, the continuous- and discrete-time models of DC-DC buck converter are given. The design procedure of discrete-time quasi-sliding mode controller is presented in the third section. The proposed quasi-sliding mode voltage-controlled converter is validated by digital simulation and the results are shown in the fourth section. The last section contains some concluding remarks.

2. QUASI-SLIDING MODE VOLTAGE CONTROLLED DC-DC BUCK CONVERTER

The schematic diagram of DC-DC buck converter with quasi-sliding mode controller is shown in Fig. 1. The proposed structure only measures sensed output voltage and it is different from most existing solutions based on measurements of voltage error and either its time-derivative or capacitor current [4].

Quasi-sliding mode control signal is compared with variable ramp signal providing a PWM signal u, which drives power switch PS. It is shown in [14] that the average dynamics of system with sliding mode control is equivalent to the average dynamics of PWM controlled system, implying that the control signal of equivalent control approach in sliding mode u_{eq} [2] is equivalent to the duty cycle control signal d of PWM controller.

The state space continuous-time model of DC-DC buck converter in the controllable canonical form, with the state variables $x_1 = \beta V_0$ and $x_2 = \dot{x}_1 = (\beta i_c)/C$ can be easily obtained from Fig. 1 in the following form:

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{b}\,u(t),$$
$$\mathbf{A} = \begin{bmatrix} 0 & 1 \\ -\dfrac{1}{LC} & -\dfrac{1}{R_L C} \end{bmatrix}, \mathbf{b} = \begin{bmatrix} 0 \\ \dfrac{\beta V_i}{LC} \end{bmatrix}, \tag{1}$$

where: L, C, R_L, V_i, and β are the inductance, capacitance, load resistance, input voltage and sensor gain, respectively. V_{ref}, V_o and βV_o are the reference, output and sensed output voltage, respectively, and $u(t)$ is 0 or 1, representing the switching state of power switch. As $u(t)$ is equal to PWM output, which corresponds to equivalent control in sliding mode control theory, we will assume that $u(t)$ is the quasi-sliding mode controller output.

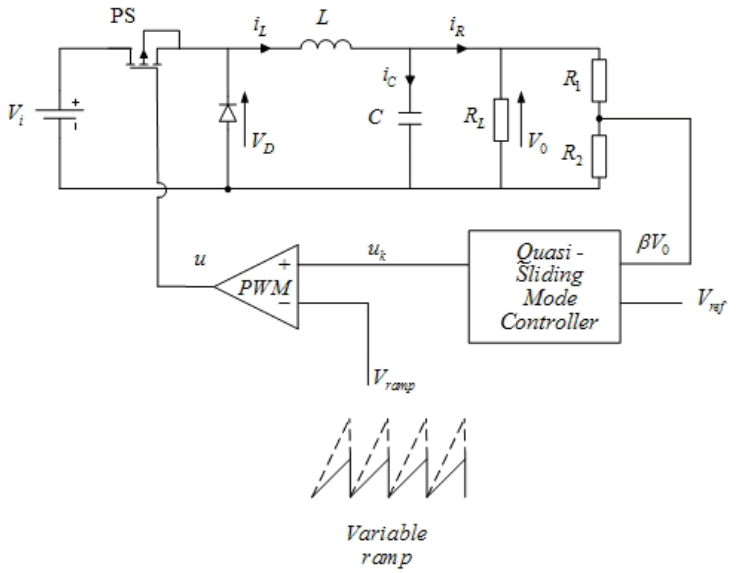

Fig. 1. Schematic diagram of quasi-sliding voltage controlled DC-DC buck converter

The main parameter perturbations are caused by variations of load resistance and input voltage and there are no external disturbances in this model. The values of the state variables x_1 and x_2 may be determined by measuring sensed output and the capacitor current i_c. To avoid the current acquisition, we suggest implementation of discrete-time sliding mode control algorithm based only on the input/output measurements. Starting from (1), the transfer function of DC-DC buck converter can be written as:

$$W_{bc}(s) = \frac{Y(s)}{U(s)} = \frac{\dfrac{\beta V_i}{LC}}{s^2 + \dfrac{1}{R_L C}s + \dfrac{1}{LC}}, \tag{2}$$

where $Y(s) = X_1(s) = \beta V_o(s)$. Under the assumption that control signal is constant during the sampling period T, $u(t) = u(kT)$, $kT \le t < (k+1)T$, the input-output model of the system in z-domain is obtained from (2) in the next form:

$$y(k) = \frac{z^{-1}B(z^{-1})}{A(z^{-1})}u(k)\,, \tag{3}$$

where $\bullet(k) = \bullet(kT)$ and:

$$A(z^{-1}) = a_0 + a_1 z^{-1} + a_2 z^{-2}\,, \tag{4}$$

$$a_0 = 1,\ a_1 = -2e^{-aT}\cos\omega_0 T,\ a_2 = e^{-2aT}\,, \tag{5}$$

$$B(z^{-1}) = b_0 + b_1 z^{-1}\,, \tag{6}$$

$$b_0 = \frac{k}{a^2 + \omega_0^2}(1 - e^{-aT}\cos\omega_0 T)\,, \tag{7}$$

$$b_1 = \frac{k}{a^2 + \omega_0^2}(e^{-2aT} - e^{-aT}\cos\omega_0 T)\,, \tag{8}$$

$$k = \frac{\beta V_i}{LC},\ a = \frac{1}{2R_L C},\ \omega_0 = \sqrt{\frac{1}{LC} - \frac{1}{4R_L^2 C^2}}\,. \tag{9}$$

z^{-1} is the unit delay i.e. $z^{-1} = e^{-pT}$, where p denotes a complex variable. The control objective is to maintain the sensed output voltage $y(k) = \beta V_o(k)$ stable, constant and equal to some constant reference voltage $V_r(k) = V_{ref}$, despite the variations of load resistance R_L and input voltage.

3. CONTROL DESIGN PROCEDURE

The algorithm, implemented in voltage control of DC-DC buck converter, is the combination of the discrete time sliding mode control and the well-known minimum variance control technique [11, 15]. The result is the quasi-sliding mode based minimum variance control, based only on input-output signal measurements, which gives better system steady state accuracy and chattering alleviation.

The design goal is to find a control $u(k)$ that will force switching function:

$$s(k) = C(z^{-1})(y(k) - V_r(k))\,, \tag{10}$$

to its minimum value (zero value in the ideal case), i.e. that will keep system motion in the vicinity of sliding surface $s(k) = 0$, determined by the quasi-sliding domain S. $C(z^{-1}) = c_0 + c_1 z^{-1} + c_2 z^{-2}$ is a polynomial with all zeros inside the unit disc. The system output in steady state is defined by:

$$y(\infty) = V_{ref} + \frac{s(\infty)}{C(1)}\,. \tag{11}$$

Therefore, the system accuracy depends on the accuracy of switching function $s(k)$, so that the smaller $s(k)$ is, the better precision is achieved. To achieve the design task, we use the control law in the form of:

$$u(k) = -\frac{F(z^{-1})y(k) - C(z^{-1})V_r(k+1) + \frac{\alpha T}{1-z^{-1}}\text{sgn}(s(k))}{E(z^{-1})B_n(z^{-1})}, \tag{12}$$

where $E(z^{-1})$ and $F(z^{-1})$ are polynomials obtained as the solutions of Diophantine equation:

$$E(z^{-1})A_n(z^{-1}) + z^{-1}F(z^{-1}) = C(z^{-1}), \tag{13}$$

$$E(z^{-1}) = e_0 = c_0 / a_0^n, \; F(z^{-1}) = f_0 + f_1 z^{-1}, \tag{14}$$

$$f_0 = c_1 - e_0 a_1^n, \; f_1 = c_2 - e_0 a_2^n. \tag{15}$$

$A_n(z^{-1})$ and $B_n(z^{-1})$ are polynomials with nominal converter parameters i.e.:

$$A(z^{-1}) = A_n(z^{-1}) + \Delta A(z^{-1}), \tag{16}$$

$$B(z^{-1}) = B_n(z^{-1}) + \Delta B(z^{-1}), \tag{17}$$

with $\Delta A(z^{-1})$ and $\Delta B(z^{-1})$ denoting polynomials with perturbed converter parameters. Notice that the relay component of the control sgn($s(k)$) is filtered through the discrete-time integrator. It is proved in [16] that the sum of all positive and negative values of sgn($s(k)$) is equal to zero when the system is in the quasi-sliding mode. Consequently, the control signal should be smooth and equal to some average value proportional to the time-interval of reaching phase. This should result in chattering reduction. Theoretically, chattering free control law can be obtained if $T \to 0$.

The implementation of (12) in (3) yields:

$$\begin{aligned} &E(z^{-1})B_n(z^{-1})A_n(z^{-1})y(k) = -E(z^{-1})B_n(z^{-1})\Delta A(z^{-1})y(k) + \\ &+z^{-1}B(z^{-1})(-F(z^{-1})y(k) + C(z^{-1})V_r(k+1) - \frac{\alpha T}{1-z^{-1}}\text{sgn}(s(k))). \end{aligned} \tag{18}$$

By adding $E(z^{-1})A_n(z^{-1})\Delta B(z^{-1})y(k)$ to both sides of (18), one yields:

$$\begin{aligned} &B(z^{-1})C(z^{-1})(y(k+1) - V_r(k+1)) = -B(z^{-1})\frac{\alpha T}{1-z^{-1}}\text{sgn}(s(k)) + \\ &+E(z^{-1})(A_n(z^{-1})\Delta B(z^{-1}) - B_n(z^{-1})\Delta A(z^{-1}))y(k+1). \end{aligned} \tag{19}$$

Polynomial $B(z^{-1})$ has its root always inside the unit disc in z-domain as, according to (7) and (8), $b_1 < b_0$. Therefore, (19) can be rewritten as:

$$s(k+1) = s(k) - \alpha T\,\text{sgn}(s(k)) + \frac{Q(z^{-1})}{B(z^{-1})}(y(k+1) - y(k)), \tag{20}$$

where:

$$Q(z^{-1}) = E(z^{-1})(A_n(z^{-1})\Delta B(z^{-1}) - B_n(z^{-1})\Delta A(z^{-1})). \tag{21}$$

Equation (20) describes the dynamics of switching function. According to (10), the system is stable if quasi-sliding mode exists in the vicinity of $s(k) = 0$, i.e. if $s(k)$ converges to and stays in bounded quasi-sliding manifold. We will now show that difference $y(k + 1) - y(k)$ is always limited by the appropriate choice of polynomial $C(z^{-1})$.

Theorem 1: *If polynomial:*

$$P(z^{-1}) = B(z^{-1})C(z^{-1}) + E(z^{-1})(B_n(z^{-1})\Delta A(z^{-1}) - A_n(z^{-1})\Delta B(z^{-1})), \tag{22}$$

has all its roots inside the unit disc for a priori known and bounded system parameter variations $\Delta A(z^{-1})$ *and* $\Delta B(z^{-1})$, *then there exists a positive real number* $\Upsilon \in R$ *satisfying:*

$$|y(k+1) - y(k)| < \Upsilon, \tag{23}$$

for every k.

Proof: Having in mind that $V_r(k + 1) = V_r(k) = V_{ref}$, difference $y(k + 1) - y(k)$ can be defined directly from (19) as:

$$y(k+1) - y(k) = -\frac{B(z^{-1})}{P(z^{-1})}\alpha T \operatorname{sgn}(s(k)). \tag{24}$$

It is obvious from (24) that $y(k+1) - y(k)$ is upper bounded (23), if $P(z^{-1})$ is Jury's polynomial. In the case of limited system parameter perturbations, the stability of $P(z^{-1})$ can be ensured by the adequate selection of stable polynomial $C(z^{-1})$.

If (23) is satisfied then there exist a positive real number $\Lambda \in R$ so that:

$$\max\left|\frac{Q(z^{-1})}{B(z^{-1})}(y(k+1) - y(k))\right| < \Lambda, \tag{25}$$

since $B(z^{-1})$ is stable polynomial. To provide stable switching function dynamics, i.e. to ensure the existence of quasi-sliding mode, the parameter α should be chosen according to the following Theorem 2.

Theorem 2: *If parameter* α *satisfies the following inequality* [15]*:*

$$\alpha T > \Lambda, \tag{26}$$

where Λ *is determined by* (25), *then there is an integer number* $K_0 = K_0(s(0))$ *so that system trajectory enters quasi-sliding manifold S, determined by:*

$$S = \{s(k) : | s(k) | < \alpha T + \Lambda\}, \tag{27}$$

and stays in it for every $k > K_0$.

Proof: First, we will prove that $s(k)$ enters the domain S in finite time, and, then, show that $s(k)$ remains in that area. Suppose that $(s(k))$, defined by (20), is a positive sequence. The proof is similar when $(s(k))$ is a negative sequence. Then:

$$s(k+1) - s(k) = -\alpha T + \frac{Q(z^{-1})}{B(z^{-1})}(y(k+1) - y(k)) < -\alpha T + \Lambda < 0, \tag{28}$$

is valid if (26) is satisfied, i.e. $s(k+1) < s(k)$ and:

$$0 < \frac{s(k+1)}{s(k)} = q(k) < 1 . \tag{29}$$

There exists a positive number δ satisfying the following inequality:

$$\left| s(k+1) - s(k) \right| = \left| s(0) \left(\prod_{i=0}^{k-1} q(i) \right) (q(k) - 1) \right| < \delta , \tag{30}$$

as $\prod_{i=0}^{k-1} q(i) < 1$ and $q(k) < 1$. Therefore, based on Cauchy's theorem of sequence convergence, we conclude that sequence ($s(k)$) is convergent. The convergence domain of sequence ($s(k)$) is:

$$\overline{S} = \{ s(k) : | s(k) | > \alpha T + \Lambda \} . \tag{31}$$

Namely, (29) implies:

$$0 < \left(\alpha T \operatorname{sgn}(s(k)) - \frac{Q(z^{-1})}{B(z^{-1})} (y(k+1) - y(k)) \right) \Big/ s(k) < 1 , \tag{32}$$

directly giving (31) for both positive and negative sequence $\left(s(k) \right)$.

Let us show that system trajectory enters domain S in finite time. Sequence ($s(k)$) converges in the domain $\overline{S}$, so it is limited, i.e.: $\lim_{k \to \infty} s(k) = s(\infty)$. Assume that $s(0) > \alpha T + \Lambda$ is satisfied. According to (20):

$$s(k) = s(0) - \sum_{i=0}^{k-1} \left(\alpha T - \frac{Q(z^{-1})}{B(z^{-1})} (y(k+1) - y(k)) \right) . \tag{33}$$

Suppose that $s(k)$ never enters the domain S. When $k \to \infty$, we can obtain the following inequality straightforward from (33):

$$\sum_{i=0}^{\infty} \left(\alpha T - \frac{Q(z^{-1})}{B(z^{-1})} (y(k+1) - y(k)) \right) < s(0) - \alpha T - \Lambda , \tag{34}$$

implying that the series $\sum_{i=0}^{\infty} (\alpha T - (Q(z^{-1})(y(k+1) - y(k))) / B(z^{-1}))$ is convergent, and its general element $\alpha T - (Q(z^{-1})(y(k+1) - y(k))) / B(z^{-1})$ converges to zero as $i \to \infty$, i.e.:

$$\alpha T = \lim_{i \to \infty} \left(\frac{Q(z^{-1})}{B(z^{-1})} (y(i+1) - y(i)) \right) , \tag{35}$$

which is opposite to the condition (26) of Theorem 2. Therefore, the assumption that $s(k)$ never enters the domain S is false. The proof is similar for $s(0) < -\alpha T - \Lambda$. Moreover, $s(k)$ enters the domain S at $k = K_0$, determined by:

$$K_0 = \text{int}((|s(0)| - \alpha T - \Lambda)/(\alpha T - \Lambda)) + 1 . \quad (36)$$

We will now show that for every $k > K_0$, $s(k)$ remains in the domain S. Let $s(K_0) \in S^+ = \{s(k): 0 < s(k) < \alpha T + \Lambda\}$. Then, according to (20), we have:

$$-\alpha T - \Lambda \underset{(26)}{<} s(K_0) - \alpha T + \frac{Q(z^{-1})}{B(z^{-1})}(y(K_0+1) - y(K_0)) = s(K_0+1) \underset{(26)}{<} 2\Lambda \underset{(26)}{<} \alpha T + \Lambda , \quad (37)$$

and $s(k)$ do not leave domain S. This is also true when $s(K_0) \in S^- = \{s(k): -\alpha T - \Lambda\} < s(k) < 0\}$ since:

$$-\alpha T - \Lambda \underset{(26)}{<} -2\Lambda \underset{(26)}{<} s(K_0+1) = s(K_0) + \alpha T + \frac{Q(z^{-1})}{B(z^{-1})}(y(K_0+1) - y(K_0)) \underset{(26)}{<} \alpha T + \Lambda . \quad (38)$$

The case when $s(K_0 + 1) < 0$ and $s(K_0 + 1) \notin S$ for $s(0)$, $s(K_0) > \alpha T + \Lambda$ is not possible as:

$$\begin{aligned} s(K_0+1) &= s(K_0) - \alpha T + \frac{Q(z^{-1})}{B(z^{-1})}(y(K_0+1) - y(K_0)) > \\ &> \Lambda + \frac{Q(z^{-1})}{B(z^{-1})}(y(K_0+1) - y(K_0)) > 0 . \end{aligned} \quad (39)$$

The case when $s(K_0 + 1) > 0$ and $s(K_0 + 1) \notin S$ for $s(0)$, $s(K_0) < -\alpha T - \Lambda$ cannot happen as well, since:

$$\begin{aligned} s(K_0+1) &= s(K_0) + \alpha T + \frac{Q(z^{-1})}{B(z^{-1})}(y(K_0+1) - y(K_0)) < \\ &< -\Lambda + \frac{Q(z^{-1})}{B(z^{-1})}(y(K_0+1) - y(K_0)) < 0 . \end{aligned} \quad (40)$$

Therefore, we have proven that $s(K_0 + 1) \in S$ and, by using the mathematical induction method, we can generalize it to:

$$s(K_0 + p) \in S , \quad (41)$$

for every positive integer number p. Having demonstrated that (41) is satisfied if (26) is valid, the proof ends.

The overall system stability is ensured if and only if the conditions of the next Theorem 3 are fulfilled.

Theorem 3: *The system described by* (3), (10) *and* (12) *is stable if and only if:*

1) *inequality* (26) *is satisfied for every* k, *i.e., quasi-sliding mode exists in the system, and*
2) *polynomial* $C(z^{-1})$ *has its roots inside the unit disk in z-plane.*

Proof: If the parameter α is chosen to satisfy inequality (12), then, according to Theorem 2, the quasi-sliding mode exists in the domain S. Now, we can see from (10) that $y(k)$ will converge to the constant reference voltage V_{ref} if and only if the polynomial $C(z^{-1})$ is stable.

4. SIMULATION RESULTS

The digital simulation has been performed to verify the proposed quasi-sliding mode voltage controller for buck converter. The parameter values are given in Table I.

The controller parameters have been set as: the sampling period $T = 50$ μs, $C(z^{-1}) = 1 - 1.067z^{-1} + 0.2846z^{-2}$, $V_{ref} = 2.5$ V, the switching and sensor gains $\alpha = 200$ and $\beta = 0.2083$, respectively.

Figure 2 shows the sensed output voltage (βV_o) waveform for the "nominal" load taken into account during the design process. With the maximum load, when the load resistance is equal to $R_{L\min}$, the proposed quasi-sliding mode voltage controller provides robust buck converter output voltage response, depicted in Fig. 3. Finally, Fig. 4 presents the output voltage signal in the most relax situation when the load resistance is $R_{L\max}$.

Table 1. Buck Converter Parameter Values

Description	Parameter	Nominal value
Input voltage	V_i	24 V
Capacitance	C	1500 μF
Inductance	L	1000 μH
PWM switching frequency	f_s	200 kHz
Minimum load resistance	$R_{L(\min)}$	3 Ω
Maximum load resistance	$R_{L(\max)}$	24 Ω
Average load resistance	R_L	13.5 Ω
Desired output voltage	V_{od}	12 V

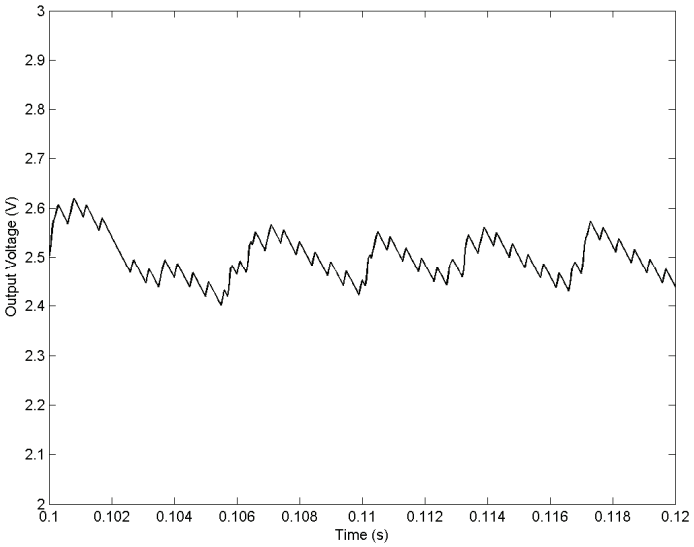

Fig. 2. Waveform of sensed output voltage for $R_L = (R_{L\min} + R_{L\max})/2$

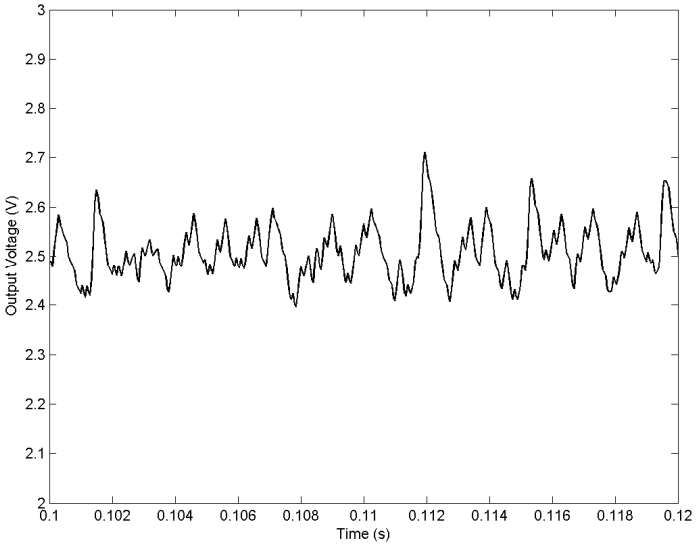

Fig. 3. Waveform of sensed output voltage for $R_{L\min}$

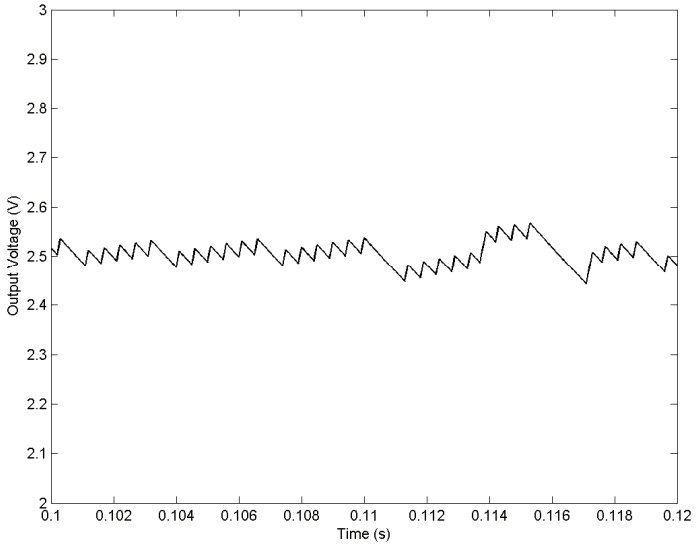

Fig. 4. Waveform of sensed output voltage for $R_{L\max}$

5. CONCLUSION

The main objective of the paper is to briefly present one approach to control of DC-DC buck converter using discrete-time quasi-sliding mode controller in combination with minimum variance control. The adopted control strategy is very appropriate for the digitally controlled power converter and for the system requirement accomplishments. The proposed quasi-sliding mode controller ensures high output voltage accuracy in the presence of parameter perturbations, which is verified by digital simulation results. Furthermore, filtering the switching control component through the discrete-time integrator reduces chattering. The control algorithm is based only on measuring the output voltage signal, rejecting the use of expensive additional current sensors in that way. It is reasonable to expect certain performance degradation in practical implementation of the proposed quasi-sliding mode voltage controlled buck converter, due to PWM nonlinearities, finite measuring precision, noise and other imperfections.

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