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GENERATING DRIVING SIGNALS FOR THREE PHASES INVERTER BY DIGITAL TIMING FUNCTIONS

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Abstract. This paper describes a new approach of generating driving signals for three phases inverters. The Pulse Position Modulations are used instead standard Pulse Width Modulation signals as driving signals. The simplicity and reliability in driving power switchers in inverters are the results of described approach. The Field Programmable Gate Array (FPGA) as high frequency PWM inverter controller is suitable for using in this approach. Presented controller has three basic blokes: numerically controlled oscillator, amplitude modulator and PWM timer. Direct Digital Synthesis (DDS) of PWM signal using sine lookup table provides three pairs of centre based, dead time adjusted driving signals. PWM signal has duty cycles in the range 0.5% to 99.5% with 8-bit resolution at switching frequency up to 100 kHz. All three parameters of the output waveform: frequency, phase and amplitude are defined and controlled by digital words. Controller has serial data interface to the host processor and as a peripheral block minimizes the conventional software overhead in generating the PWM waveforms. In the stand-alone mode of operation, two-chip solution, which includes FPGA and A/D converter, is applied as a control block in the three phase fixed frequency DC/AC converter

Key words: Inverter, pulse width modulation, pulse position modulation, FPGA, direct digital synthesis.

1. Introduction

Modern production of power switching transistors provided power conversion at ultrasonic frequencies (> 20 kHz). It gave an opportunity for developing DC/AC converters with higher efficiency; higher power packaging density, lower output voltage distortion and lower spurious signal level

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in the audio frequency band. There are many reasons for moving towards a completely digital control system in an inverter application. The switching signals for the three- phase power converter are digital rather than analogue in nature. They may be produced using analogue comparators but are just as easily generated using digital timing functions. Digital approach offers the most flexible control system. The frequency, phase and amplitude of generated waveform can be numerically controlled with high resolution and accuracy. PWM pulses are precisely dead time adjusted, what is required to prevent cross conduction in the inverter power devices. The realization of a completely digital control also reduces the susceptibility of the system to the noise sources associated with the power converter.

2. Description of topology

The inverters, very important types of power electronics devices, are used as an irreplaceable part of uninterruptible supplies or an asynchronies motor's control device. The inverter is consisting by power circuit and control circuit. The configurations used in inverters are half bridge or full bridge configurations. The full bridge topology is shown in Fig. 1.

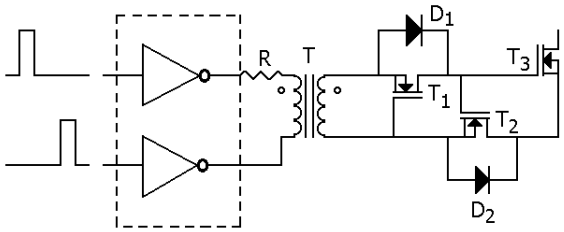


Fig. 1. Full bridge topology.

The switching component (MOSFET, IGBT) in Fig. 1 is driven by pulse width modulated (PWM) signals. The ratio between ON time (T_{on}) and period of switching frequency (T), named δ factor, is the essential characteristic of PWM signal. The switching frequency is in range of few tenth kHz. The modulating signal is voltage sinusoidal signal which frequency is in range of 10 Hz to 100 Hz. In inverters that are parts of uninterruptible supply the frequency is 50 Hz. In inverters for motor driving the frequency and amplitude are both changeable (one of them or both). The inverter generate PWM square signal from input DC signal by turning on or turning off switching component. This signal, going trough low pass filter (L and C

on Fig. 1) became a sinusoidal voltage signal. The amplitude of sinusoidal voltage signal is zero if the value of δ factor is 0.5. The value of output voltage increases proportion until the value of δ factor increase to maximum (value 1). In this point the sinusoidal voltage signal has it's maximum and it is equal to value of input DC voltage. If the transformer is used instead of wounded component the output voltage is proportional to input voltage with transformers ratio. The value of output voltage decreases proportion until the value of δ factor decrease to minimum (value ≈ 0). In this point the sinusoidal voltage signal has it's minimum and it is equal to negative value of input DC voltage.

The drains of transistors T_1 and T_3 are connected with positive port of input DC voltage. However, potential between gait and source has not constant value. It means that is necessary adaptive circuit to connect with control circuit. The most often solution is pulse transformer. However in this situation is needed to satisfay volt – second balans. The volt – second balans is equality between productions of current's amplitude and T_{on} period and productions of Voltage's amplitude and T_{off} period. Today, the MOSFET is used as switching component. It needs a 2 V voltage, minimum, on gait to be in ON state. This value depending on each component. So it can be possible make sure ON state with 4 V on gait. On another side, voltages higher than 20 V on gate generate a breakthrough the isolating film between gait and channel. The maximal modulation is limiting by these conditions in range ($\delta_{max} \leq 0.6$). It means that the amplitude of output sinusoidal voltage couldn't be higher than 60% of DC input voltage.

There are many procedures for solution this problem. The particular driving circuits for T_1 and T_3 is one of possible solution. In this case there are two driving circuit, each for both transistors. These driving circuits are connected with control circuit over optocoupler. The complexity is a disadvantage of this configuration. The new type of controller is in usage today. The main disadvantage of this solution is not exiting of galvanic isolation.

In Fig. 2 is shown a driving circuit. With this configuration the modulation became a 100% with galvanic isolation. Only if the transistors are MOSFET, the solution is applicable. The MOSFET needs a PWM driving signal. The MOSFET's input impedance is in order of 100 kΩ, and input capacitance, C_{gs}, is in order of 100 pF. The impulse on C_{gs} that will charge it is qwait enough to put MOSFET in ON state. The MOSFET's ON state is stating until then capacitance C_{gs} discharged. So, the information about start and end go PWM impulse is impotent. The impulses which are gen-

erated in this way named a Pulse Phase Modulation (PPM) impulses. The impulse charges the capacitance C_{gs} over the diode D_1. The duration of impulse is determined by MOSFET's input capacitance. While the capacitance C_{gs} is charge the MOSFET will be in ON state. The opposite polarity impulse will turn off the transistor T_1. In this way T_1 cross-connecting gait and source of T_3 and put it in OFF state. There is a possibility that the some noise signals change the MOSFET's state. The diode D_2 and transistor T_2 has a role to increase reliability switching. The capacitance gait source will be charge to opposite value than was in ON period. The role of transistor T_1 is the same like the transistor T_2 but in period turning off.

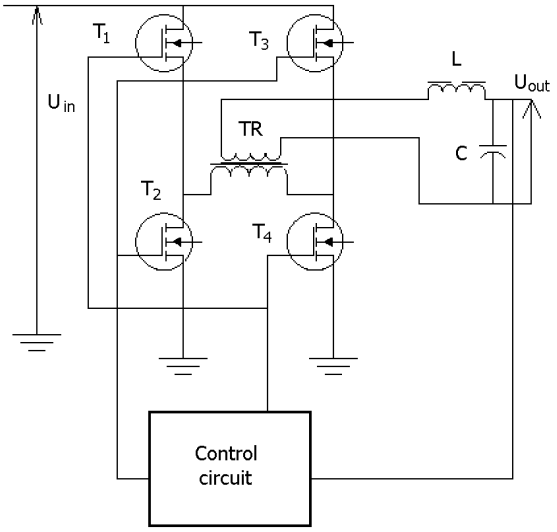


Fig. 2. Driving MOSFET circuit.

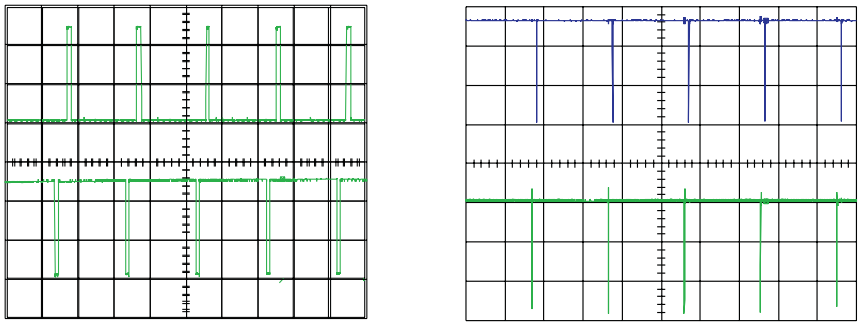
In respecting with opposite polarity of impulses (demagnesation of transformer core is done in very switch cycle) there is no possibility of transformer's saturation. Theoretical, the 100% modulation became possible. Regarding to the duration of charging and discharging impulses the 99% modulation is under real expectation.

Differencing the PWM impulse is the most simplicity way to get driving impulse. By this way it can be possible to get only driving edges. The reliability of this solution is low because there are parasitic impulses.

The much better solution to generate the signal is to use digital timing functions. The frequency and amplitude of generated waveform can be nu-

merical controlled with high resolution and accuracy. On Fig. 3a is shown a PWM signal that is generating by digital timing functions. The waveform with minimal δ is shown up, and the waveform with maximal value of δ is shown down.

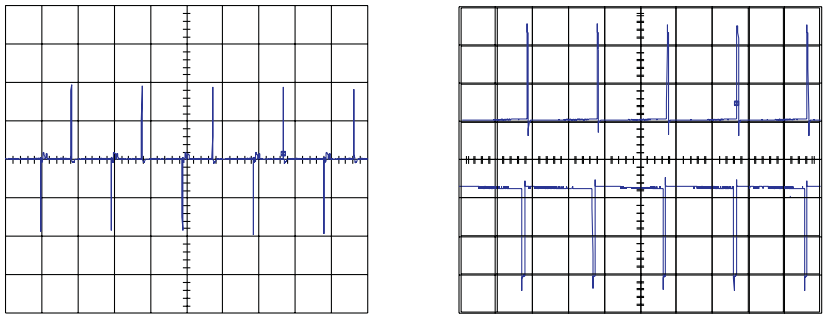
The impulses that are corresponded that PWM signal's edges are shown on Fig. 3b. The signals are generated with digital timing functions. The waveforms on primary side of transformer are shown on Fig. 4a.



a) b)

Fig. 3. a) PWM impulse generated by used digital time functions.
b) The impulses that are corresponded that PWM signal's edges.

The waveform of regenerating PWM signal between gate and source of power MOSFET is shown on Fig. 4b.



a) b)

Fig. 4 a) PPM signal on primary side of transformer.
b) Regenerating PWM signal between gate and source of power switch.

The realized inverter output signal waveform is shown on Fig. 5. up figure presents output PWM signal waveform. Down figure presents output sinusoidal waveform (behind output low–pass LC filter with boundary frequency 300 Hz).

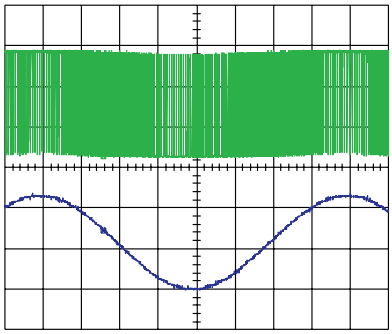


Fig. 5. Realized inverter output signal waveform.

3. Generating PPM Signal Using Digital Timing Functions

The continuous signal waveform can be represented by series of Pulse Width Modulated (PWM) samples instead of Pulse Amplitude Modulated (PAM) samples. Conversion of PAM pulse into PWM pulse is shown at Fig. 6.

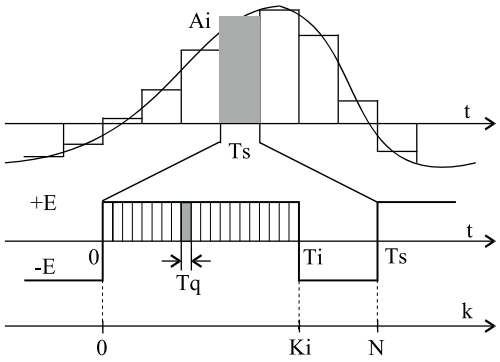


Fig. 6. Conversion of PAM into PWM pulse.

Both pulses have same volt-second product. Amplitude E of bipolar PWM pulse is constant, while its duration is linear function of PAM pulse amplitude A_i:

$$T_i = \frac{T_s}{2}\left(1 + \frac{A_i}{E}\right), \qquad |A_i| \leq E \tag{1}$$

The cycle of PWM signal T_s can be uniformly divided in N timing intervals, quantization periods T_q, which are the basic parts in digital synthesis of PWM pulse. In that way, PWM pulse with duty cycle in the range 0–100% can be represented by integer number from 0 to N. By substitutions $T_i = K_i T_q$ and $T_q = T_s/N$ in equation (1) we get relation between amplitude of PAM pulse A_i and duration of PWM pulse expressed by K_i, the number of quantization periods:

$$K_i = \frac{N}{2}\left(1 + \frac{A_i}{E}\right), \qquad |A_i| \leq E \tag{2}$$

The PWM sample is coded with n bits, so we have relation $N = 2^n$. As the number of bits is increased, the resolution of PWM signal is also increased, but it requires higher quantization frequency $F_q = 1/T_q$. Assuming that pulse duration errors are uniformly distributed [2], signal to quantization noise ratio is:

$$\frac{S}{N} = 6n \text{ [dB]} \tag{3}$$

If voltage drops in inverter power switches and interpolating Low Pass (LP) filter may be neglected, then we can use eq. (2) for calculation of PWM samples for different modulating signal waveforms (sine, ramp, saw-tooth ...). For example, analytical expression for sine modulated PWM samples is:

$$K_i = \frac{N}{2}\left(1 + h\sin\left(\frac{2\pi}{M}i + \Theta\right)\right), \qquad i = 1 \ldots M \tag{4}$$

where $h = A/E$ equals the ratio of sine and PWM pulse amplitudes, which we will define as index of modulation of PWM signal. Frequency of modulating signal is F_s/M, where $F_s = 1/T_s$ is sampling frequency and M equals the number of PWM samples per cycle of the generated signal. The initial phase of the generated signal is Θ.

The equation (4) explains how we can control amplitude, phase and frequency of generated signal. Amplitude control is performed by changing the index of modulation. Unmodulated PWM signal ($h = 0$) has duty cycle of

50%, and output voltage is zero. For $h = 1$, duty cycle of PWM signal vary in the range 0 to 100%, and amplitude of generated signal is equal to PWM pulse amplitude.

Frequency of generated signal can be controlled by changing sampling frequency or the number of samples M per cycle of output signal. A varying of sampling frequency is not advised because the switches and LP filter in inverter power device are selected and adjusted for one single frequency. By changing the number M, it is possible to have fine frequency resolution in wide range of frequencies at lower clock frequency needed for digital synthesis of PWM pulse.

Accumulating phase changes at sampling frequency can generate DDS works on the principle that digitized waveform of a given frequency. The phase changes in time are linear function and therefore the frequency of generated signal will be constant. Digital accumulators are excellent generators of linear progression of digital numbers. The phase value is added each period of sampling clock. The resulting instantaneous phase value is then applied to the sine lookup table once during each clock cycle. The phase to amplitude conversion occurs in the sine lookup ROM. The generated frequency F_g and sampling frequency F_s are related to the phase increment value $\Delta\Phi$ by the following equation:

$$F_g = \frac{F_s}{2^L}\Delta\Phi \tag{5}$$

where L equals the number of bits in the phase accumulator. Frequency resolution is $\Delta f = F_s/2^L$. Any frequency can be generated by programming the phase increment within the bit resolution of the phase accumulator. As the output frequency is increased the number of samples per sinusoid is decreased. Since sampling theory states that at least two samples per cycle are required to reconstruct the output waveform, maximum generated output frequency is $F_s/2$. For $\Delta\Phi = 0$ constant output voltage is generated, which value depends on current contents of phase accumulator and index of modulation.

This method provides soft frequency changes because of continuous phase accumulating, and there is no strong harmonic signal generation due to transition period. The changes of instantaneous phase of signal are performed by accumulating determined phase increment in one or a few sampling periods.

All the sinusoidal amplitude information necessary for a complete 360° cycle is contained in one quarter of cycle. Therefore, only 90° of mapping are required in the lookup table. The phase accumulator simply clocks in

both directions and then reverses sign of amplitude for the other half period. This allows more economy in the lookup table ROM. Number of memorized samples is trade off between desired phase resolution and available ROM capacity. Therefore only most significant part of the phase accumulator is used as address pointer on lookup table. This reduced number of bits is called phase truncation. The truncation of phase applied to the lookup table introduces jitter in the output waveform that is observed as spurious responses. In general, these spurs will be no lager than $6(P+2)$ [dB] below desired output, where P is the number of phase bits applied to the lookup table. [3].

4. Description of Controller

The controller has two mode of operation. It can work as a stand-alone controller and as a PWM peripheral block in an inverter or AC motor control system. The main part of controller is single chip FPGA. Whole arithmetic and timing functions are realized by digital hardware. The FPGA core program and sine lookup table are loaded from 8 pins serial ROM through the serial port and an advantage of this approach is that PCB is very similar to that for a final ROM coded device.

As PWM peripheral block, controller minimizes the conventional software overhead in generating the PWM waveforms. Once initialized, all that is required to change the parameters of generated signal is to update some registers. Phase, frequency and amplitude of generated signal are controlled by host processor through the Serial Peripheral Interface (SPI). Control bits are clocked into shift register, and on a receipt of a whole data word, they are buffered in Phase Increment Register (PIR), Amplitude Control Register (ACR) and Timer Control Register (TCR). The ACR and PIR controls amplitude, phase and frequency of generated output voltage. The TCR is used to program PWM frequency, the dead time and pulse deletion time (shortest pulse width).

In the stand-alone mode of operation, controller is modified by adding Analog to Digital Converter (ADC). Analog input signal is converted in digital form and then is used instead of ACR contents. It gives a possibility of autonomous regulation of output voltage amplitude. However, phase and frequency changes in this mode of operation are not possible. One such realization of controller is applied in three-phase inverter that generates AC voltage of constant frequency 50 Hz. It will be presented in this chapter, but generality of consideration about choice of parameters will not be reduced. Fig. 7. shows a block diagram of controller.

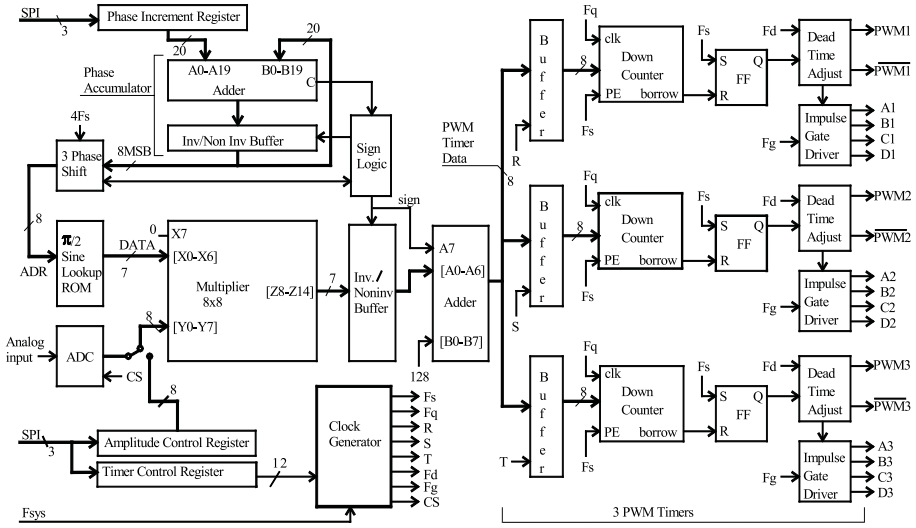


Fig. 7. Functional block diagram of controller.

All three parameters of the waveform: frequency, phase and amplitude are defined by digital words. Frequency resolution is determined by L, the number of bits in the phase accumulator. Phase resolution is determined by P, the number of bits applied to the ROM lookup table. Amplitude resolution is determined by n, the number of bits in the PWM timer.

The number n we can choose from 8 to 12. For an inverter application it is usually enough to select value $n = 8$, what gives by eq. (3) the signal to noise ratio of 48 dB.

The number of bits in phase accumulator is $L = 20$. Let frequency resolution of the generated signal has the exact value $\Delta f = 0.1$ Hz. Thus resulting PWM signal frequency will be $F_s = \Delta f 2^L = 104.86$ kHz, and quantization frequency is $F_q = F_s 2^n = 26.844$ MHz, what is below the highest system clock rate. For the generated waveform frequency of 50 Hz, PIR must be programmed with phase increment value 500.

Maximum frequency of generated output voltage is trade off with LP filter complexity and desired attenuation of switching harmonic frequency. For example, forth order LP filter with cut off frequency $F_s/4$ will attenuate fundamental frequency of PWM signal for at least 50 dB, thus ripple voltage peak to peak will be 0.3% of PWM pulse amplitude.

For selected value $P = 8$, the phase resolution equals $90/2^P = 0.35$ degrees. The 8 Most Significant Bits (MSB) of phase accumulator are input to the phase shift block which sequence generates three addresses for sine lookup table in every cycle of PWM signal. Applying $h = 1$ to Eq. (4) and using only the sine factor then leads to form for calculation of lookup table data:

$$K_i = 128 \sin\left(\frac{2\pi}{1024}\right), \qquad i = 1 \ldots 256 \tag{6}$$

Only one quarter of cycle is mapped to ROM. The samples are coded with 7 bits. Additional sign logic block generates MSB of PWM sample (0 = plus, 1 = minus). The lookup table requires 256×7 bits of memory.

The analog input signal to ADC is positive error voltage that is equal to difference of output voltage and its nominal value. Start of analog to digital conversion is synchronized to generated output signal period, so the error signal is sampled always at same phase instant. The sampled value is holding through the whole signal period, so the influence of error voltage ripple to output voltage regulation is reduced.

In this application 8 bits ADC is used. The measurement error is less then 0.5% of full-scale voltage at analog input. Digital information is represented in offset binary format.

Amplitude modulation of PWM samples can be realized by placing a digital multiplier between the lookup table and timer circuit. Digital multiplier and adder realize the next arithmetic operation:

$$Z = X\frac{Y}{256} + 128 \tag{7}$$

where X is the PWM sample from lookup table and Y is digital output word from ADC. Two-quadrant 8×8 bits multiplication is performed in time interval $T_s/4$, what is about 2.5 μsec. 8 LSB of the product are not used and in this way dividing by 256 is performed. PWM samples are scaled by factor $Y/256$ that has value in the range 0 to 255/256. Thus the index of modulation is varied in the range nearby 0 to 1, and consequently amplitude of generated output voltage is changed from zero to DC supply voltage. As analog input voltage to ADC is increased, the index of PWM modulation and amplitude of AC output voltage are also increased.

By adding $N/2 = 128$ to result of multiplying we get numeric value of PWM sample in offset binary format. Multiplying and offset adding operations are performed in time-sharing mode for all three-phase signals

in one PWM cycle. The computed values are then set apart in three timer data buffers. Parallel entry to down counters and flip-flop (FF) setting is done with rising edge of sampling signal Fs. The counters are decremented with quantization clock frequency. When they reach zero state, flip-flops are reset and so we obtain three pairs of center based., sine modulated PWM driving signals. However, some extra features have been added to broaden the range of possible applications. The gate drive block was added to allow interface to transformer coupled gate drive for MOSFET and IGBT circuits. [4].

Timer control register defines the dead time, shortest PWM pulse width and gate drive impulse width. A dead time, which can be set to $J \cdot 150$ ns, $J = 1, 4, 16$ and 64, is required to prevent cross conduction in the inverter power devices. The gate drive impulses width can be programmed in the same ranges as dead time. The pulse deletion time is the shortest high or low pulse that will be generated and prevents unnecessary switching losses and extra-induced noise.

5. Conclusion

This paper describes modern approach to realize inverter. The primary target was to produce a highly integrated device, which also had the flexibility to meet the requirements of a wide range of applications. This integrated device was implemented to realize inverter. The technical characteristics of inverter are: duty ratio from 0.5% up to 99.5%. The path taken has been to first develop the peripheral functions set on a single device and to subsequently move on to a single integrated device.

The next stage of integration is outlined in which whole controller will be designed as an Application Specific Integrated Circuit (ASIC). This will provide a truly cost effective, single chip solution for wide range of DC/AC converter and motor control applications.

REFERENCES

1. The Programmable Logic Data Book: *XILINX*. 1994.
2. Q2334 DDS Data Sheet: *Qualcomm*. 1991.
3. The DDS Handbook: *Stanford Telecom*. 1994.
4. Transformer Isolated HEXFET Driver: *International Rectifier*. Application note 950A, 1985.