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LABORATORY MODEL OF THE COMPENSATED SYSTEM FOR DISSEMINATION OF STANDARD SIGNALS VIA SATELLITE

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Abstract. This paper describes the laboratory model of the proposed compensated system for dissemination of standard time and frequency signals via TV satellite. The circuit for analog delay of the order of 250 ms, which corresponds to the satellite uplink plus downlink propagation delay, was realized with three cascaded Matsushita MN3005 analog delay integrated circuits. Testing of the laboratory model, combined with computer simulation of the PLL with propagation delay included, show that there are ranges of PLL parameters for which PLL is stable in spite of large propagation delay. This proves that the proposed compensated system will operate satisfactorily.

Key words: Laboratory model, Compensated system, Dissemination, TV satellite, PLL stability.

1. Introduction

Dissemination of standard time and frequency signals with high accuracy has a great importance for clock comparison and frequency source calibration, time scale coordination, telecommunications, etc. The broadest possibilities for transmission are offered by geostationary TV satellites because a wide area is relatively uniformly covered by a single transmitter (a satellite's transponder). Standard signals are inserted in an unused TV line of the vertical blanking interval. The major drawback concerning time and frequency dissemination via TV satellite is the satellite diurnal motion

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around its nominal geostationary orbital position, resulting in both propagation delay variations and Doppler shift which limit accuracy of received standard signals (extracted from TV signal). For example, Doppler shift at the received standard frequency is of the order of 10^{-8} [1], [2], while propagation delay variation is of the order of 100 μs [2].

If standard frequency only is to be disseminated via TV satellite, Doppler shift can be automatically compensated to a large extent by applying a compensation method described in [1], [3] which is performed in a TV studio itself and was tested practically. An externally synchronized synchronizing pulses generator in a TV studio, an uplink transmitter, a TV satellite, and a satellite receiver in a TV studio are parts of a PLL. The reference (standard) frequency input to the PLL (TV line frequency, 15625Hz) is derived from the atomic frequency standard. Such a way of dissemination assures high accuracy of the received standard frequency - TV line frequency - and it is easily multiplied to several MHz.

However, the aforementioned method does not allow high accuracy of the received standard time signals - second pulses - inserted in TV line 10 because of the propagation delay of about 250 ms. A complex method of compensation which enables accurate both standard time and frequency signals dissemination via TV satellite is proposed in [4]. Doppler shift compensation is performed by the PLL, as in [1], [3]. In addition to that, composite synchronizing pulses of a video signal are phase shifted in order to achieve coincidence between the second pulses from the atomic clock and TV line 10. Intentionally delayed second pulses are then inserted in TV line 10, assuring that the received second pulses coincide with the second pulses from the atomic clock.

The method proposed in [4] was not experimentally verified. TV authorities are reluctant to allow experiments since it may impair the TV picture quality. If PLL parameters (ω_n and ζ) are not adequately chosen, then phase steps for phase shifting of the composite synchronizing pulses may force the PLL out of lock or introduce instability. It will certainly cause temporary loss of the color subcarrier synchronicity, which must be avoided. Because of that, testing of the proposed method and determination of adequate values of PLL parameters must be performed on a laboratory model.

This paper will describe the laboratory model of the compensated system for dissemination of standard signals via TV satellite. Detailed testing of the laboratory model, combined with computer simulation of the PLL with propagation delay included, will reveal PLL transient behavior caused by phase steps and help determine the most adequate PLL filter, i.e. PLL parameters (ω_n and ζ).

2. The Laboratory Model

The compensated system for dissemination of standard signals via TV satellite, proposed in detail in [4], requires an expensive equipment: the frame synchronizer, the atomic frequency standard and clock, the time interval counter, etc. Several electronic circuits, developed specially for this purpose, are also required. However, the laboratory model can be realized in a very simple way since most of the expensive equipment and specialized circuitry are no longer needed, except for the time interval counter. It should be mentioned that circuits for generation and delaying of the second pulses, to be inserted in the video signal, are no longer necessary since they are not critical for the model operation. In addition to that, the ZNA134 in-chip sync pulses generator is not necessary in the model since it can be completely replaced by 2.5625 MHz VCXO (Voltage Controlled Crystal Oscillator).

The most difficult problem was to realize circuit for the analog delay of the order of 250 ms which is equivalent to the satellite uplink plus downlink propagation delay. By using elementary trigonometry, it may be calculated that the propagation delay lies in the range of 240 ms-280 ms. For Belgrade latitude, where the uplink transmitter is located, the propagation delay is approximately 253 ms. The analog delay circuit was realized with three cascaded Matsushita MN3005 MOS analog delay integrated circuits.

The block diagram of the laboratory model is given in the Fig. 1. Blocks drawn with thick lines are critical for the model operation. The 10 MHz high precision sine wave crystal oscillator is in fact the HP10544A, the OCXO internal time base of the HP5370A time interval counter, the output of which is buffered and also used as a reference frequency output of the HP5370A. The sine to square wave (TTL) shaping is done by a LSTTL NOR logic gate. The TV line frequency (15625Hz) the phase of which may be adjusted, used as a reference frequency in the method proposed in [4], is obtained at the output of the line frequency divider combined with the adjustable delay circuit, described in detail in [4]. However, the -3 dB upper cut-off frequency of the MN3005 is approximately 6 kHz (sine wave). Because of that, TV line frequency cannot be used as a reference frequency for PLL operation of the model. One eighth of the TV line frequency (1953.125Hz) is used instead, since it is sufficiently lower than cut-off frequency of the MN3005. So, the total frequency division ratio is $640\times8=5120$. It is realized with 74LS90 ($\div10$) and a part of CD4060 ($\div512$). The adjustable delay circuit, realized with 74LS221 monostables (160 ns and 1.6 μs) and 74LS02 NOR logic gates, provides coarse and fine delay steps of 1 μs and 100ns by simply swallowing corresponding clock pulses, [4]. Since the monostable's output is asynchronous to the clock pulses, then the phase steps in fact may

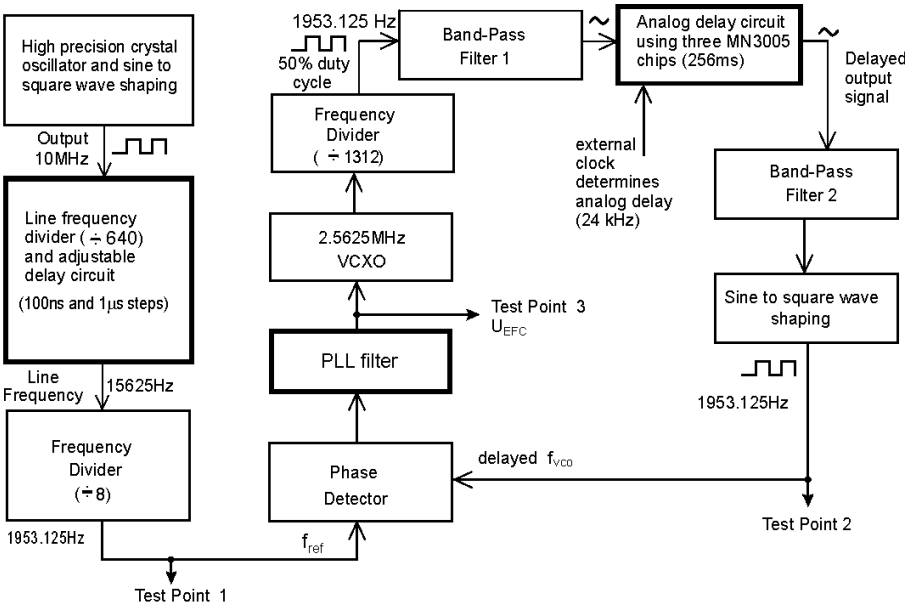


Fig. 1. Block diagram of the laboratory model of the compensated system for dissemination of standard signals via satellite.

be either 1 μs or 2 μs, and either 100 ns or 200 ns. The delay steps in the model are equivalent to phase shifting of the composite sync pulses in the proposed compensated system. In this way, $f_{ref} = 1953.125$ Hz with adjustable phase is obtained.

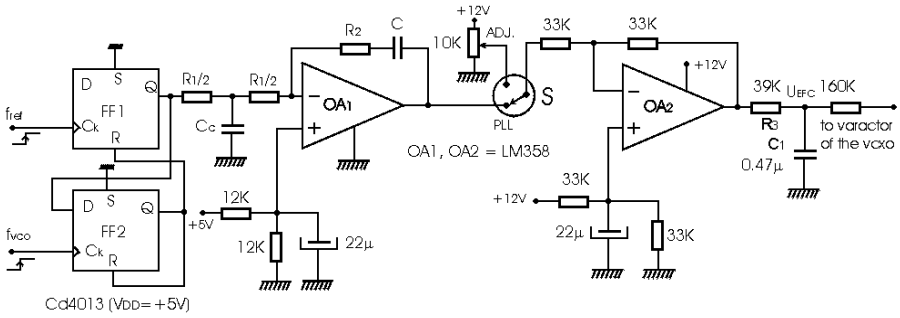


Fig. 2. Phase detector and PLL filter.

The rest of the block diagram in Fig. 1 is the PLL with propagation

delay included which is equivalent to the block diagram of the compensation method. f_{ref} is the reference frequency for the PLL. The schematic diagram of the phase detector and PLL filter of the Fig.1 is given in Fig.2. The phase detector is the edge-triggered RS flip-flop realized with two D flip-flops (FF1 and FF2) of CD4013. f_{ref} is applied to the SET input, while delayed f_{VCO} is applied to the RESET input. Q output of the FF1 is the phase detector output. Inputs and outputs of FF1 and FF2 are connected in a way which determines the priority of the SET input to switch the Q1 output always from 0 to 1, whereas the RESET input can only switch the Q1 output from 1 to 0. The operating range of such a phase detector is 2π, and its gain KPD depends on the power supply voltage VDD

$$K_{PD} = \frac{V_{DD}}{2\pi} = \frac{5}{2\pi} \tag{1}$$

The PLL filter is an active PI filter realized with an operational amplifier 1 ($OA1$), R_1, R_2 and C, [5]. C_C improves transient suppression (sharp edges of the phase detector square wave output) which leads to better PLL dynamic behavior and reduction of VCXO noise, as suggested in [6]. C_C and R_1 make a simple low-pass filter which creates an additional pole in the PLL. The OA2 is an inverter that assures a proper polarity of the U_{EFC} (voltage for electronic frequency control of the VCXO). A simple low-pass filter realized with R_3 and C_1, another additional pole, removes residual reference frequency noise from the U_{EFC} which is used to control the VCXO output frequency. It is easily derived that the PLL filter transfer function is

$$K_F(s) = \frac{1 + CR_2 s}{CR_1 s(1 + \frac{C_c R_1}{4} s)(1 + C_1 R_3 s)}. \tag{2}$$

The 2.5625MHz VCXO, built with 74HC4060, is almost identical to the VCXO described in detail in [7]. The main difference is that 2.5625MHz quartz crystal is used instead of 2 MHz crystal. The BB104G varactor is used to achieve the electronic frequency control. The VCXO output frequency increases for increasing U_{EFC}. For maximum U_{EFC} swing of $\approx$10 V, f_{VCXO} changes for $\approx$40Hz around its nominal value. Selector S, inserted between OA1 and OA2, has two positions: "PLL" for normal PLL operation, and "ADJ." for free-running operation of the VCXO and fine adjustment of nominal VCXO output frequency at $\approx$2.5625 MHz at $U_{EFC} = 4.51$ V, the center of the most linear part of the VCXO operating range. Output of the PLL is the phase of the f_{VCXO}, i.e. the integral of the f_{VCXO}. Therefore, gain of the VCXO is found as

$$K_{VCXO}(s) = \frac{K_{VCXO}}{s} = \frac{2\pi\Delta f_{VCXO}}{s\Delta U_{EFC}}, \tag{3}$$

where $K_{VCXO} = 2\pi f_{VCXO}/\Delta U_{EFC}$, in [rad/sV]. $\Delta f_{VCXO} = 9.8$ Hz, and $\Delta U_{EFC} = 1.99$ V, are increments centered around $U_{EFC} = 4.51$ V.

The VCXO output frequency is then divided down to 1953.125 Hz by the frequency divider with total division ratio of N=1312. Its gain is simply $1/N$. The total division ratio is achieved by cascading a part of 74HC4060 ($\div$16), 74HC40102 ($\div$41), and finally one half of 74HCT74 connected as a T flip-flop ($\div$2), which assures 50 % duty cycle of the 1953.125 Hz square wave (TTL), the amplitude of which is 5 V_{PP}. This signal should be then delayed by $T_D \approx$250 ms in the analog delay circuit realized with MN3005 audio analog CCD integrated circuits. MN3005 consists of 4096 cascaded SAMPLE/HOLD MOS delay cells which require a digital clock for successive shifting of the analog input signal along the cascaded cells. Delay per single MN3005 integrated circuit is calculated as $T_{D1} = 4096T_{CP}/2$, where T_{CP} is the clock pulses period. In order to achieve total delay $T_D = 256$ ms and upper -3 dB cut-off frequency of $\approx$6 kHz, three cascaded MN3005 integrated circuits are used with 24 kHz digital clock. The amplitude of the clock is the same as power supply of the MN3005, i.e. +12V. Schematic diagram of one stage of analog delay circuit is given in Fig. 3.

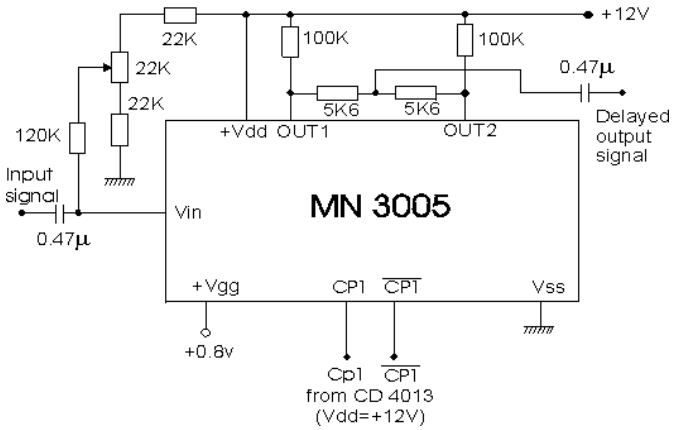


Fig. 3. One stage of analog delay circuit.

However, maximum input voltage for MN3005 is limited to ≈ 3 V_{PP}. In addition to that, the 1953.125 Hz square wave should not be directly applied to the MN3005 input because sharp edges would be distorted due to MN3005 method of operation and limited bandwidth. Therefore, a large jitter may be introduced. Because of that, 1953.125 Hz $5V_{PP}$ square wave is firstly passed through a simple two-pole active inverting band-pass filter 1 with a center frequency $f_0 \approx 1953.125$ Hz, a bandwidth of ≈ 200 Hz, and a midband gain

$A_0 \approx 0.5$. Band-pass filter 1 is realized with a TL071 single operational amplifier. A 2.5 V_{PP} sine wave is obtained at its output and then fed to the analog delay circuit. The band-pass filter delay of ≈ 33 μs, measured by an oscilloscope, is neglected. Output of the analog delay circuit is ≈ 2.5 V_{PP} sine wave distorted by a large noise originating from the 24 kHz clock. It must be passed through a band-pass filter 2, the same as band-pass filter 1 except for the midband gain $A_0 \approx 1$, in order to remove the 24 kHz noise before a sine to square wave shaping is performed, and therefore to minimize jitter. The input D.C. bias voltage of each MN3005 is adjusted for maximum output of the band-pass filter 2. The sine to square wave shaping is done with LM311 voltage comparator, and finally the delayed $f_{VCO} = 1953.125$ Hz 5 V_{PP} TTL signal is obtained.

3. Computer Simulation of the PLL

The two additional poles previously mentioned ($4/C_C R_1$ and $1/C_1 R_3$), and especially the propagation delay T_D, increase the order of the PLL and introduce instability. Therefore, the PLL parameters ω_n and ζ must be chosen carefully in order to achieve the PLL stability. Anyway, the time constant due to R_1, R_2, and C must be sufficiently greater than both the additional poles and the propagation delay T_D. Because of that, certain simplifications in the PLL could be made. Now, the PLL filter transfer function is simply $KF(s) = (1 + CR_2 s)/CR_1 s$ as in [5], [7], so the phase transfer function H(s) of the PLL is given by

$$H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \tag{4}$$

where ω_n is the natural frequency given by

$$\omega_n = \sqrt{\frac{K_{PD} K_{VCXO}}{N R_1 C}}, \tag{5}$$

and ζ is the damping factor given by

$$\zeta = \frac{\omega_n R_2 C}{2}. \tag{6}$$

For $R_1 = 36$ $k\Omega$; $R_2 = 2.2$ $M\Omega$; $C = C_C = 2.2$ μF, it is obtained that $\omega_n = 0.4868$ rad/s and $\zeta = 1.1781$. The value for damping factor $\zeta \approx 1$ is suggested in [5] for the fastest elimination of the loop error during the input phase steps. The two additional poles are two orders of magnitude higher

than calculated value for ω_n, and therefore neglected. Influence of $T_D = 256$ ms is also neglected since it is ≈ 20 times lower than the total time constant of $\approx 5\ s$.

However, in the computer simulation and stability analysis of the PLL there will be no simplifications. The MATLAB program package, used for simulation, requires open loop gain K_{OL}(s) obtained by multiplying gains of the phase detector, the PLL filter given by Eq. (2), the VCXO, the frequency divider, and the analog delay circuit (its gain is simply $\exp(-sT_D)$)

$$K_{OL}(s) = \frac{K(1+\tau_2 s)e^{-T_D s}}{\tau_1 s^2(1+\tau_3 s)(1+\tau_4 s)}, \tag{7}$$

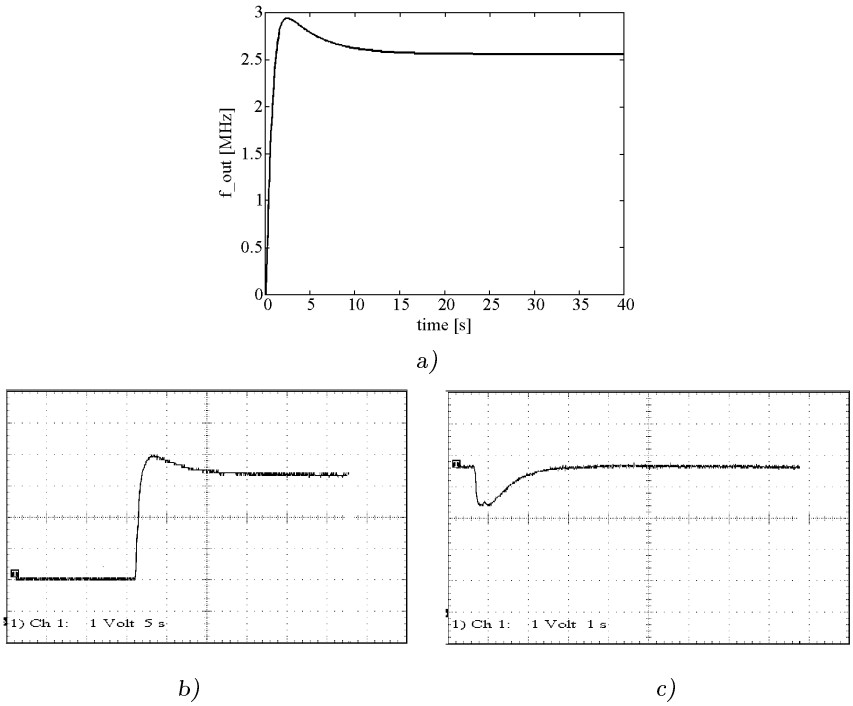
where $K = K_{PD}K_{VCXO}/N = 0.018768$, $\tau_1 = CR1 = 79.2$ ms, $\tau_2 = CR_2 = 4.84\ s$, $\tau_3 = C_C R_1/4 = 19.8\ ms$, $\tau_4 = C_1 R_3 = 18.33\ ms$.

The PLL stability analysis is performed by the root locus method for both extreme values of T_D, 240 ms and 280 ms. The analysis is firstly made for T_D=240 ms. If τ_1 is fixed, then the PLL is stable for $\tau_2 \in (0.3288\ s, 19.2010\ s)$ which results in $\omega_n = 0.4868$ rad/s and $\zeta \in (0.0800, 4.6735)$, Eq. (5) and (6). If τ_2 is fixed, then the PLL is stable for $\tau_1 \geq 0.0197$ s which results in $\omega_n \leq 0.9761$ rad/s and $\zeta \leq 2.3621$. The analysis is then made for $T_D = 280\ ms$. For fixed τ_1, the PLL is stable for $\tau_2 \in (0.3793\ s,\ 14.0343\ s)$ which results in $\omega_n = 0.4868$ rad/s and $\zeta \in (0.0923, 3.4159)$. For fixed τ_2, the PLL is stable for $\tau_1 \geq 0.0291$ s which results in $\omega_n \leq 0.8031$ rad/s and $\zeta \leq 1.9435$.

Finally, the lock-in process of the closed PLL output frequency is simulated for $T_D = 280\ ms$ (the worst case) and shown in Fig.4a. Except for the first overshoot which is unavoidable, the subsequent overshoots and undershoots are negligible, as in [5] for $\zeta \approx 1$. It proves that both the additional poles and the propagation delay T_D do not significantly influence the initially assumed values for ω_n and ζ, which are adequate for the application.

4. Experimental Results

The laboratory model operation is finally experimentally verified for $T_D = 256$ ms. The U_{EFC} voltage, i.e. the TEST POINT 3 is displayed on the TEKTRONIX TDS210 digital real-time oscilloscope. The f_{REF} is firstly disabled, the OA1 output becomes saturated at ≈ 11 V, the $U_{EFC} \approx 1$ V. After the f_{REF} is enabled, the U_{EFC} is recorded and shown in Fig. 4b. It may be seen that, due to a very low value of ω_n, it takes ≈ 15 s for the OA1 output to become non-saturated, and after that moment the lock-in process begins. Although the saturation of the OA1 is not taken into account



a)

b) c)

Fig. 4. a) *Simulation of the PLL lock-in process.*
b) *Lock-in process of the PLL.*
c) *Response of the PLL to 2 μs input phase delay step.*

during simulation, the lock-in process in Fig. 4b is practically identical to the simulation in Fig.4a. The U_{EFC}, i.e. response of the PLL to the input phase delay step of 2 μs is also recorded and shown in Fig. 4c. It may be seen that the PLL is stable, there are no oscillations in the response, and steady state is reached within a couple of seconds.

In addition to that, TEST POINTS 1 and 2 are used to start and stop the HP5370A time interval counter. In the steady-state, the HP5370A displays ≈260.57 μs. After the 2μs phase delay step, the displayed interval suddenly decreases by 2 μs since the PLL is slow, then it increases to greater than ≈260.57 μs, and finally slowly decreases to the steady-state of ≈260.57 μs. Such measurement results are in a complete accordance with the Fig. 4c.

5. Conclusion

The laboratory model of the proposed compensated system for the dissemination of standard time and frequency signals via TV satellite is described in this paper. It is the PLL with the large propagation delay in-

cluded. However, the calculated values of the PLL parameters, the PLL computer simulation and analysis, and finally the experimental results are in a complete accordance in spite of the large propagation delay. It proves that the proposed compensated system will operate satisfactorily.

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