FACTA UNIVERSITATIS (NIŠ)
Series: Electronics and Energetics vol. 12, No. 3 (1999), 65-77

UDC 621.314.57

# ONE SOLUTION OF DC/DC CONVERTER WITH ADAPTIVE FEEDBACK CONTROL

**Miroslav Lazić**

**Abstract.** The main disadvantages of converter with a digital PWM controller are slower transient response and output voltage quantization error. This paper deals with these problems and one solution of digital adaptive feedback control is proposed.

The adaptive feedback control is based on the Digitally Controlled Continually Variable Slope Delta Modulation principle. The PWM duty cycle change is proportional to the difference of two neighboring output voltage samples. The value of the duty cycle change is proportional to the slope of output voltage change. A step of duty cycle change is digitally controlled by 4 bit algorithm, so each step has one of 16 discrete values.

In this paper the comparative analyses of classic PWM converter and digital converter with uniform quantization, is described. Both converters operate at the same switching frequency and have the same loop bandwidth. A new approach of the adaptive drive signals generation is suggested with algorithm for declination of disadvantages of digital converter with uniform quantization. This type of converter is called Digital Converter with Adaptive Feedback Control.

## 1. Introduction

The digital converters are switch mode power supplies with digitally generated Pulse Width Modulation signal. So far, there are only some specific solutions in power electronics, such as power supplies controlled by a microcomputer. The main reasons for this are complex feedback control configurations, slower transient response and output voltage quantization error. Some converter configurations such as power supplies, which are made as a combination of more basic converter topologies or soft switching converter,

Manuscript received Jan. 10, 1999.

The author is with IRITEL d.d., Batajnički put 23, 11080 Belgrade, Serbia. E-mail addres is: mlazic@iritel.bg.ac.yu, .

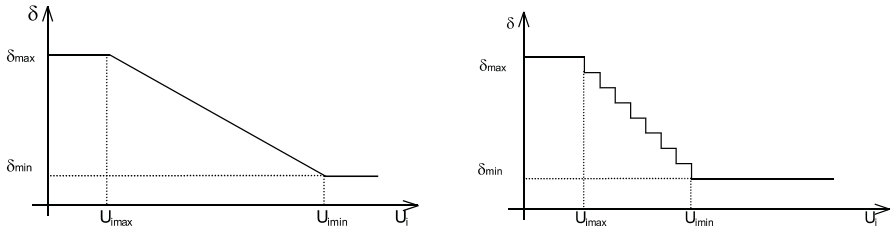
have more switching elements. The turn-on and turn-off times of power switch are dependent on each other. It means that the operating frequency of these switches is equal, but phase and duration are different. In these cases a classical solution for generating PWM signal is difficult to apply. The digital generation of a PWM signal is the logical solution. In this method all signal are generated from the same clock frequency and phase shift.

PWM signal is simple one to be realized with digital circuit. If some of FPGA circuits are used, then it is possible to apply one digital control configuration for many different topologies of PWM converters.

This paper deals with one procedure for generating PWM signals for power switches in the SMPS. The adaptive feedback control makes better dynamic response of digital converter. The value of the duty cycle change is proportional to the slope of output voltage change.

## 2. PWM Converter with Digital Feedback

The ratio between turn-on time of power switch and switching period is named $\delta$ factor. The $\delta$ factor value depends only on the input voltage change at converter without losses. It is possible to define difference between classical PWM converter and digital converter with this factor. The basic difference between classical PWM converter and digital converter is show in Figure 1.




a) b)

*Fig. 1. Generating of PWM signal with classical and digital converter*
*a) $\delta = f(U_i)$ with calassical PWM converter*
*b) $\delta = f(U_i)$ with digital PWM converter*

The minimal value of $\delta$ factor ($\delta_{min}$) is defined by the characteristics of a power switch

$$\delta_{min} \leq \frac{t_r + t_f}{T} \tag{1}$$

where $t_r$ is the rise time of power switches and $t_f$ is the fall time of power switches.

On the other side, maximal $\delta$ factor value ($\delta_{max}$) is defined by converter's topologies.

With a change of the $\delta$ factor it is possible to establish any function between input and output value only in range $[\delta_{min}, \delta_{max}]$. For example: In the constant voltage source, with the change in $\delta$ factor it possible to eliminate variation due to the input voltage.

So, for a classic PWM converter, delta factor, $\delta$, takes any value between minimum ($\delta_{min}$) and maximum ($\delta_{max}$). The change of delta factor in range $[\delta_{min}, \delta_{max}]$ is continuous. In digital converter, the change of delta factor is discontinuous. The total change of delta factor $\Delta\delta$, depends on the voltage failure $u_e$, previous value of the $PWM$ signal, feedback gain $G$, cut-off frequency $\omega$ and elementary growth of $\delta$ factor $\partial\delta$

$$\Delta\delta = f(u_e, PWM, G, \omega, \partial\delta) \tag{2}$$

Value of $\delta$ factor can be one in the array $\delta_i \in (1, 2, \ldots, n)$. The number of discrete values of delta factor is defined by bit number, which is used for output value measurement. Every value of $\delta$ factor corresponds to one value of discrete $PWM$ signal. For example: If the output value is measured with eight bits ($n = 8$) then exists $2^n = 256$ values for $\delta$ factor. If $\partial\delta$ has constant value, then converter always has equal increase. That kind of converter is reffered to as converter with uniform change of delta factor.

Converters with uniform quantization are simple for realisation. At Fig. 2 the specific output voltage waveform for the digital converter with uniform change of delta factor, is given. In this case the digital converter is without losses, with constant gain and is independent on frequency. At figure 2a is given the output voltage waveform at initial converter operation, at figure 2b step-load change recovery and at figure 2c converter in steady state operation. Disadvantages of this solution are large quatization error $Q_e$ and slow step-load change recovery time $t_s$. Quatization error depends on bit number witch are used for measurement of output value. For example: If eight bits ($n = 8$) are used for measurement of output voltage $U_o$ (nominal value of 10V), one elementary voltage quantum is

$$\partial u = \frac{U_o}{2^n} = \frac{10}{256} = 0.039V \tag{3}$$

This equation is valid only for converter without losses. In reality there are losses in inductive components and switches, so this fact must be re-

spected when this equality is used. If total power loss is 20 %, elementary voltage increase will be

$$\partial u = \frac{1.2Uo}{2^n} = \frac{12}{256} = 0.0469V \tag{4}$$

This equation does not show the change of output voltage caused by variations of the input voltage. The minimal $\partial u$ is proportional to the change of the input voltage. The nearest value of output voltage in the ideal case is in the range of $10 \pm 0.039\ V$. The increase of nominal value of the output voltage causes proportional increse of the absolute value of quantization error (quantization noise).

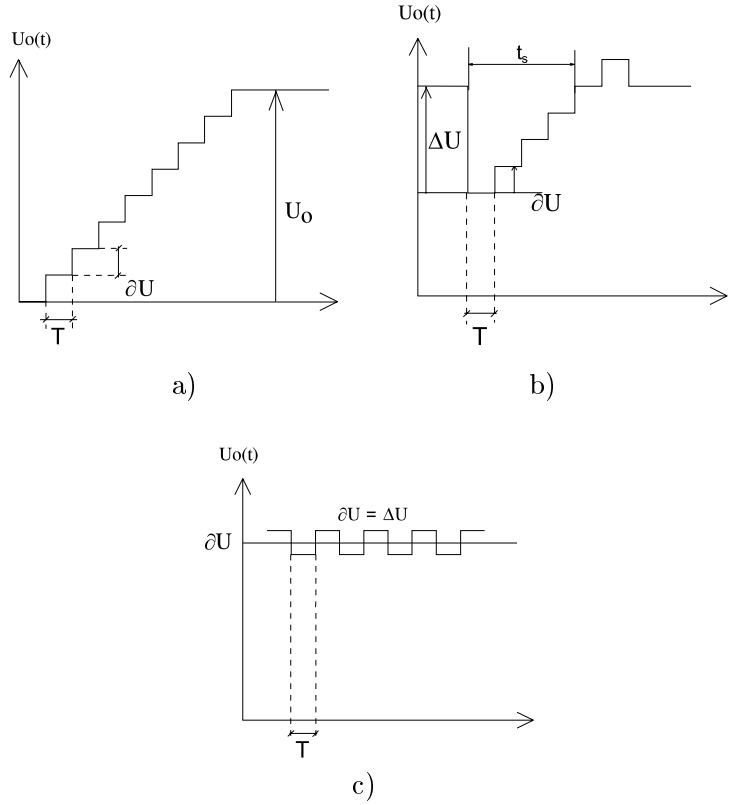



*Fig. 2. Waveform of voltage in digital converter:*
*a) soft start, b) step-load change recovery,*
*c) steady state operation*

The output voltage error $\Delta U$, increases for amount $\partial u$ in each period $T$. Delta factor is changed for one elementary growth $\partial\delta$. If output voltage was

decreased by $\Delta U$, then it is necessary for $\Delta U/\partial u$ period to reach nominal value of output voltage. The step-load change recovery time is given by

$$t_S \geq \frac{\Delta U}{\partial u} T \tag{5}$$

It is obvious that the step-load change recovery time of digital converter with uniform change of delta factor depends on value of the elementary growth of delta factor $\partial\delta$. If decreasing of step-load change recovery time is desirable, it is necessary to expand elementary growth of delta factor. On the other hand this will cause proportional increasing of quantization noise. The result of computer simulation for one digital converter with uniform change of delta factor is given in Figure 3.

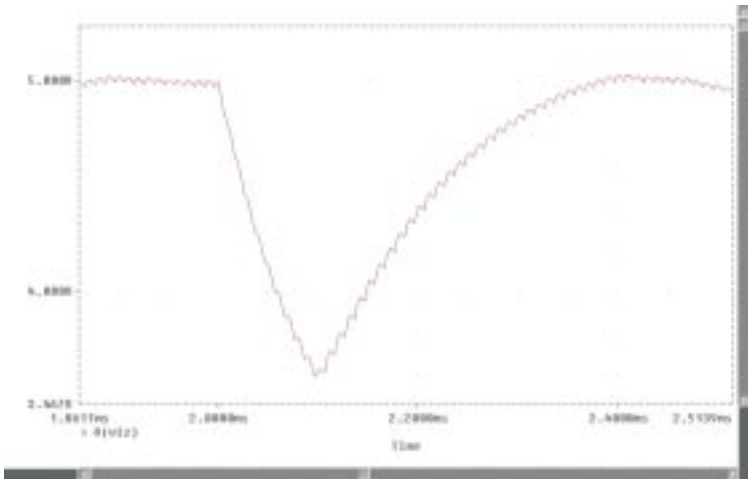
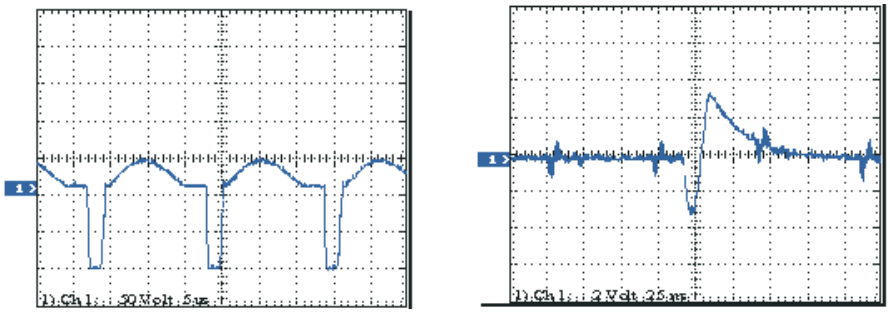


*Fig. 3. Step load response for digital converter with uniform change of delta factor obtained by PSPIC simulation*

The waveform of voltage across the power switch and load voltage for one digital converter with uniform change of delta factor is given in figures 4a) and 4b), respectively. The converter is in use in the locomotive electropneumatics brakes control. The technical charateristics of this converter are: nominal value of input voltage $U_i = 110$ V, $U_o$: defined by an elektropneumatic brake force from 30 V to 120 V, $P_{max}$: 500 W, $f_s$: 20 kHz, $n$: 8 bits, $Q_e$:$\approx 1$ V. Topology is forward.

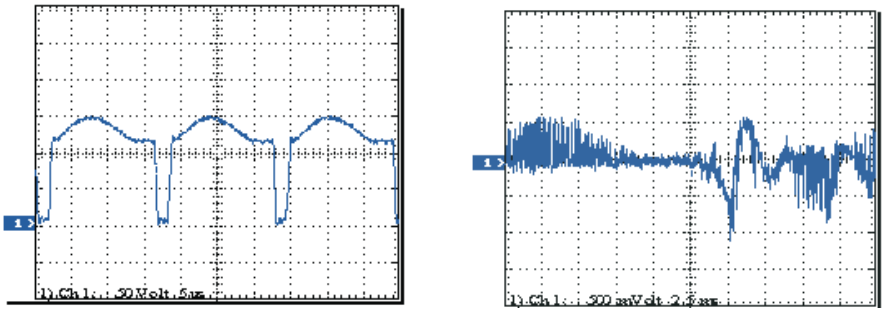
The waveform voltage of power switch and load voltage for one classic PWM converter with continual change of delta factor is given in figures 5a) and 5b), respectively.

The digital converter and classic PWM converter has the same elements of power electronics circuits (forward topology) and diferent elements of feedback control. The waveforms of power switch voltage before step load are shown in figures 4a) and 5a). The both waveforms are evidently identical which is result of the same power circuit.



a) b)

*Fig. 4. Voltage waveform of power switch and load voltage for digital converter*



a) b)

*Fig. 5. Voltage waveform of power switch and load voltage for PWM converter*

The value of step load is increase from 10 % to 100 % of maximum output power. In both cases the input voltages have equal values and are independent from load. The results of measurements of three parameters (output

voltage recovery time $t_S$, output undervoltage $U_{UV}$ and output overvoltage $U_{OV}$) are shown in Table 1.

Table 1

| | $t_S$ [ms] | $U_{OV}$ | $U_{UV}$ [V] |
|---|---|---|---|
| Digital converter with uniform change of $\delta$ factor | 70 | 3.5 | 3.5 |
| Clasical $PWM$ convertor | 7.5 | 0.5 | 1 |

The dynamic charateristic of digital converter with uniform change of delta factor can be significantly better if algorithm of operation is changed. The relation between elementary growth $\partial\delta$ and error voltage can be established as

$$\partial\delta = f(u_e) \tag{6}$$

Hence, $\partial\delta$ depends on value of the output voltage error. If the error is greater, the elementary growth $\partial\delta$ increase proportionaly. This converter is called the digital converter with adaptive feedback control. Figure 6. shows characterstic output voltage waveform of digital converter with adaptive feedback control.

It can be seen that the step-load change recovery time and quantization error are reduced. In this approach, the difference between reference value and instantaneuous value of output voltage is measured. The sign of difference causes increasing or decreasing of $PWM$ signal for elementary growth $\partial\delta$. Therefore, the absolute value of output voltage is not followed, but only amount of voltage error. This approach is well known in telecommunications as Delta Modulation. Basic rewards of Delta Modulation is simple realisation. If calculation of $\partial\delta$ depends on amount of output error, such procedure is called Adaptive Delta Modulation. Therefore, when output voltage error is detected, the difference between reference and instantaneous value of output voltage increases. The amount of elementary growth $\partial\delta$, is changed, too. When the sign of difference between reference and instantaneous value of output voltage was changed, then sign and amount of growth is changed, too. Therefore, both, amount of output error and trend of $\partial\delta$ change are controlled.

Fig. 7 shows simplified principal scheme of the Adaptive Delta Modulator used in feedback of a digital converter.

Control electronic is composed of comparator which compares reference and output voltage. Output of the comparator is set at logic "1" when the

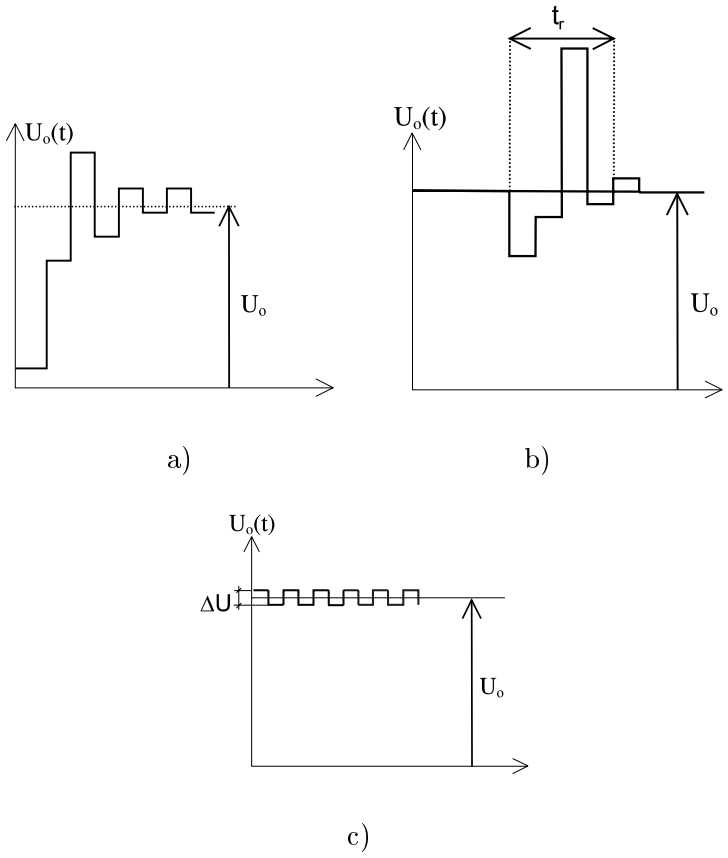



*Fig. 6. Waveform of output voltage digital converter with adaptive feedback control: a) soft start, b) step-load change recovery, c) steady state operation.*

output voltage is greater then the reference one. Contrary is set at logic "0". Logic criteria is taken from the comparator output to the input of adder. Criteria defined by sign of $\partial\delta$ change in previous period $t_{i-1}$, is taken to the another input of adder

$$\text{Sign}\partial\delta = 1, \forall\delta_t = \delta_{t-1} + \partial\delta \tag{7}$$

$$\text{Sign}\partial\delta = 0, \forall\delta_{t\_} = \delta_{t-1} - \partial\delta \tag{8}$$

It means that if $\delta$ factor is increased in $t_i$ moment, with respect of $\delta$ factor in $t_{i-1}$ moment, an adder input takes logic "1". If $\partial\delta$ was decreased, an adder input is at logic "0". If signals of different logic level are taken as adder

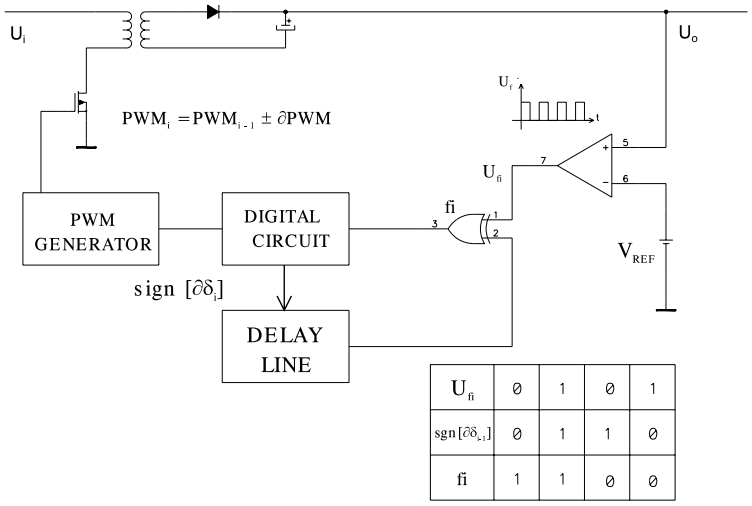



*Fig. 7. Simplified sheme of digital converter with adaptive adjusment of $\partial\delta$*

inputs then steady state is provided. It means that the one adder output is generated logic "0". This signal provides changes of $\delta$ factor for amount of $\partial\delta$ in opposite direction with respect of previous moment. Therefore, if $\delta$ factor was increased in $t_{i-1}$ moment for $\partial\delta$ and there is an increase of output voltage for $\partial u$ in $t_i$ moment, then $\delta$ factor will be decreased in $t_{i+1}$ moment for amount of elementary growth $\partial\delta$. Hence, in steady state conditions, output voltages varies between value $U_{\text{nominal}} \pm \partial u$. But it is important that when adaptive procedure is applied, equations (3) and (5) are not valid. Growth $\partial u$ produces maximum amount of enabled noise in the output voltage. Logic "1" at adder output shows that error exists and it should be removed. Change of $\delta$ depends on a mount of error and length of logic "1" row which appear on adder output. There is digital logic in feedback, composed of memory unit which remembers sign of change $\partial\delta$ in some previous periods. The $\delta$ factor change is accommodated to the length of symbol row by same sign. This paper describe solution in which last four bits are remembered

$$\Delta\delta = f(\text{Sign}\partial\delta_{t-1}, \text{Sign}\partial\delta_{t-2}, \text{Sign}\partial\delta_{t-3}, \text{Sign}\partial\delta_{t-4}) \tag{9}$$

Function $f(\text{Sign}\partial\delta_{t-i})$ is chosen so that good dynamic response of converter is obtained. Figure 8 shows different output voltage waveforms of the digital converter for different values of function $f(\text{Sign}\partial\delta_{t-i})$.

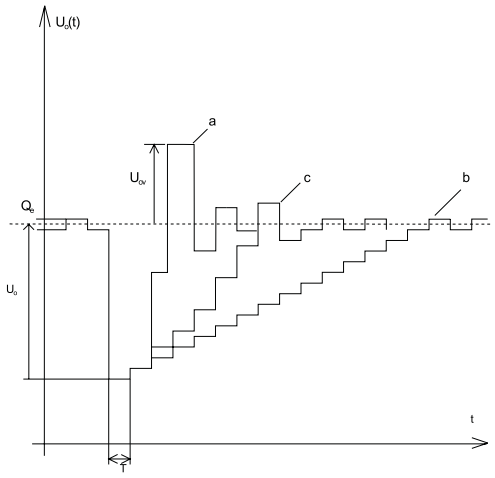



*Fig. 8. Step recovery response of digital converter for diferent shapes of function* $\partial\delta = f(u_e)$

Figure 8a shows output voltage waveform when overcompensated digital feedback was applied. It can be seen that slope of $\delta$-factor change function is too large. It means that rise time is short and step of change of $\delta$-factor is large. Output voltage has reached reference voltage for short time, but both exeeding Uov, and damping time $t_r$ exist. Otherwise, there is under-compested feedback (figure 8c). In this case rise time of output voltage is large. The main disadvantage of this solution is poor step load change recovery response. Beetwen this two bad cases, there are number of "good" solutions. By changing the parameters of function (given by equations 9), feedback parametars of digital power supplies could be optimized. Figure 8 shows idealized output voltage waveforms. In this idealized case bandwidth of feedback loop is wide. Response depends on other parameters of feedback (amplification, cut-off frequency, damping factor). However, procedure for optimization is the same for both, idealized and real configuration.

Practical solution of the previously described procedure is simple. Last four bits are stored in a shift register and form address for lookup table. The content of that memory is programmed algorithm for predicted change of current duty cycle growth $\partial\delta$.

## 3. Operational Algorithm

The algorithm of operation for the digital converter is shown in Fig.9. During steady state operation, the delta factor is alternatively increased and

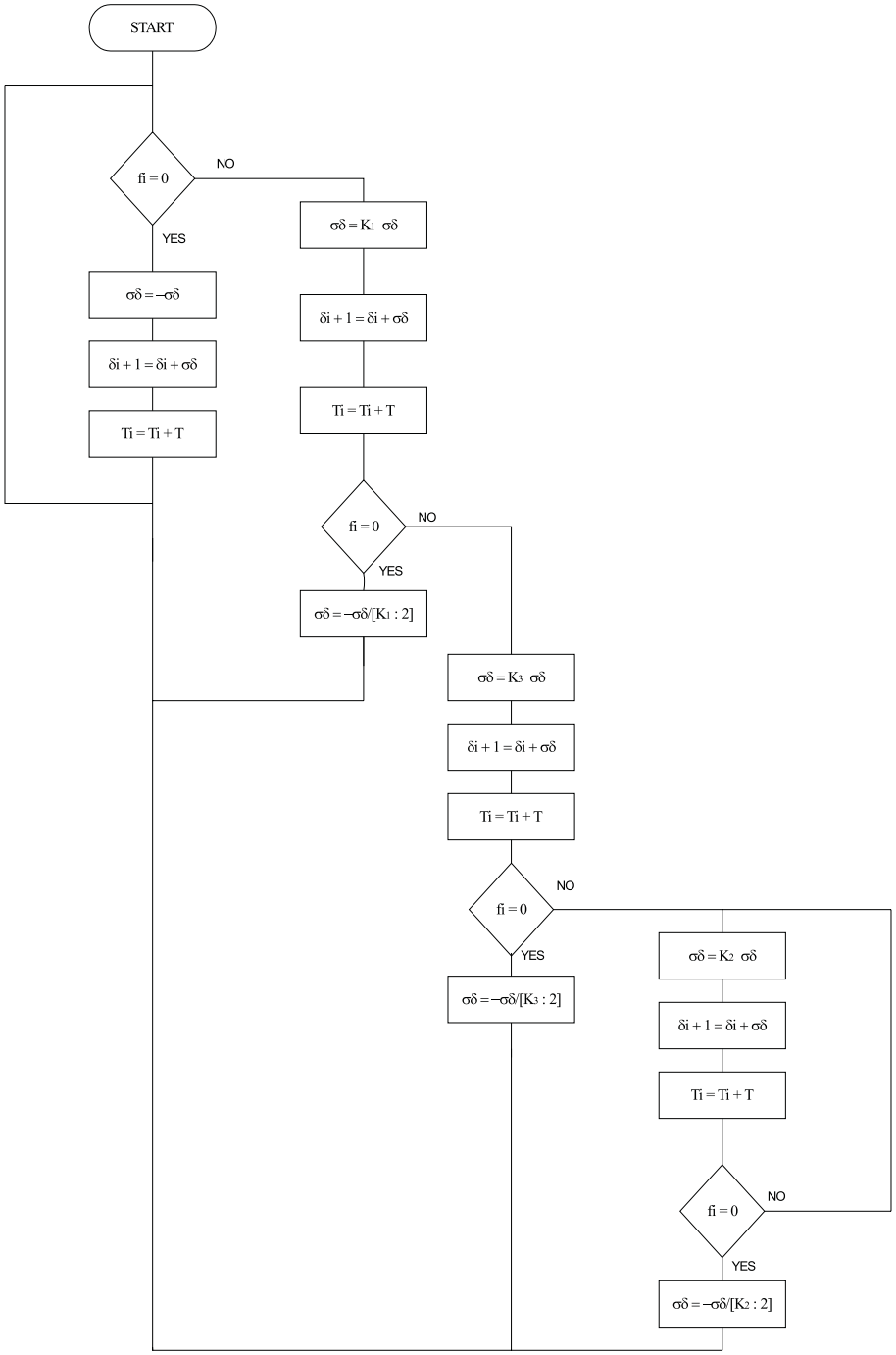



*Fig. 9. Algoritahm of operation*

decreased. When two consecutive "ones" exist, the change of the delta factor increases K1 times and the direction of the change remains. If such an increased delta factor causes the unit to reach the output voltage (i.e. the error signal changes its polarity), the direction of the delta factor change reverses and its absolute value decreases to 50%. If there are three consecutive "ones", delta factor changes K2 times. The longest array that is recorded consists of four "ones" and that leads to the highest change in the delta factor.

Digital converters with the adaptive change of the delta factor have a shorter step-load change recovery time than the digital converters with the uniform change of the delta factor. On the other hand, the disadvantage of the adaptive control is that overshoot due to the sudden change of the delta factor exists. With the uniform delta factor change the overshoot cannot be higher than one elementary step of the change. However, by proper selection of the **Ki** coefficients, dynamic specifications could be changed. There is always a trade off between the response time and the overshoot. The overshoot could be eliminated by using an additional feedback network, at a price of loosing one of the basic advantages of the described method – simplicity.

## 4. Conclusion

This paper describes an approach to the digital generation of the driving signals for $PWM$ switchmode converters. Drawbacks of the digital converters with the uniform delta factor change are analyzed. In this paper comparative analyses of the classic $PWM$ converter and digital converter with uniform quantization is presented. The results of comparative analyses are given in Table 1. The classic $PWM$ converter's dynamic characteristics are much better than digital converter's with uniform change of delta factor. A new approach of an adaptive drive signals generation is suggested. The basic idea of adaptive method is that change of duty cycle's elmentary growth is in function with value of output voltage error. The greater errors can be eliminated faster if duty cucle's elementary growth is proportional to the output voltage's value. There are many topologies of digital converters with adaptive feedback control. Increasing overvoltage on the output is the result of decreasing of step load recovery time. So the optimization is necessary. The feedback gain and frequency characteristics are parameters which must be included in optimization. The number of bits in memory is also one of criteria for optimization. This paper is initially one for many papers which deals with the problems of digital converter with adaptive feedback control. The digital converter with an adaptive feedback control which is easy for

realization with better dynamic characteristics than digital converter with uniform change of delta factor will be final result of these researches. The presented approach is intended for realization in a programmable logic circuit. This way is simple and reliable configurations for the control stage of the digital converter are easily achievable.

## REFERENCES


1. Skender M., Lazić. M. and Sasic B.: *All Digital High Frequncy PWM Inverter Controler.*, Powersystem World '96. conference & exibit, Las Vegas, Nevada, 1996.
2. Lukatela G., Drajić D., Petrović G.: *Digital telecomunications.*, Belgrade 1978.
3. Severns R.P., Bloom G.E.: *Modern DC-To-DC Switchmode Power Converter Circuits.*, Van Nostrand Reinhold Computer Science and Enginering Series, New York, 1985.
4. Chryssis G.C.: *High - Frequncy Switching Power Supplies, theory & desing.*, Mc-Graw - Hill Publishing Company, New York, 1989.
5. Erikson R.: *Fundamentals of Power Electronics.*, Boulder Colorado, 1996.