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SIMULATION OF TIME–DELAY EFFECTS IN ULTRA-HIGH SPEED AMPLIFIERS WITH NEGATIVE FEEDBACK

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Abstract. The paper describes the simulation of delay times of high speed amplifiers in microstructures. Beyond the current standard of about 10GB/s ringing and instability–problems increase in data amplifiers with an negative feedback within a stage. There are three causes for instability of the closed loop gain: (1) a not real feedback gain (g_{fb}) by the combined parasitic effects of line inductances and stray capacitances (2) too many poles (n) of the inner gain (g_i) and (3) too large delay times (t_d). Let us assume: $n = 1$ and concentrate on time delays. Results will be given in the case of an unity–gain–amplifier and a current–to–voltage converter with an inner transistor amplification of $g_{i,DC} = 10$, a cut–off frequency of $f_o = 10$GHz.

1. Introduction

The paper describes the simulation of delay times of high speed amplifiers in microstructures. Beyond the current standard of about 10 GB/s ringing and instability-problems increase in data amplifiers with an negative feedback within a stage. The regarded open loop transmission gain (g_{lt}) is

$$g_{lt} = \frac{g_{fb} g_{i,DC} e^{(-2\pi f t_d)}}{(1 + j\frac{f}{f_0})^n}$$

with: g_{fb} = feedback gain, g_i = inner gain with multiple poles n, t_d = delay time.

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1. Theory of Negative Feedback–controlled Circuits

The principle problem can be described by the simulation of negative feedback structures. Figure 1 shows the schematic circuit diagram of a closed-loop amplifier.

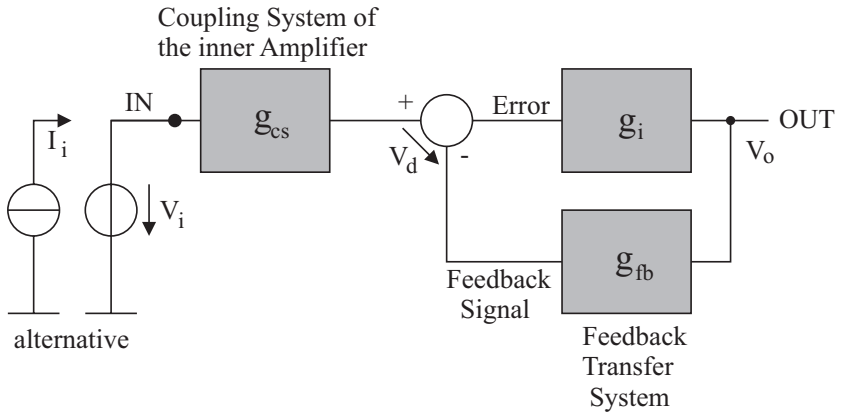


Fig. 1. Schematic circuit diagram of a closed-loop amplifier

The closed-loop gain is given by

$$A = g_{cs}\frac{g_i}{1 - g_{fb}g_i} \tag{1}$$

with

$$g_{cs} = \frac{V_d}{V_i}\Big|_{V_o=0} \quad \text{and} \quad g_{fb} = \frac{V_d}{V_o}\Big|_{V_i=0}$$

This amplification of closed-loop systems can be normalized by the idealized gain under the condition of infinite inner gain g_i

$$A_\infty = \lim_{g_i \to \infty} A = -\frac{g_{cs}}{g_{fb}} \tag{2}$$

The normalized closed-loop gain is

$$\begin{aligned}\frac{A}{A_\infty} &= \frac{1}{1-\dfrac{1}{g_{fb}g_i}} \\ &= \frac{1}{1-\dfrac{1}{g_{lt}}} = E_F\end{aligned} \tag{3}$$

The relation between the real and the desired amplification is given by the error factor (EF), which depends only on the loop transmission gain: $g_{lt} = g_{fb}g_i$ with g_{fb} as a complex transfer function of the feedback network and the inner amplification factor g_i:

$$g_i = \frac{g_{i,DC}e^{-2\pi f t_d}}{(1+j\dfrac{f}{f_o})^n} \tag{4}$$

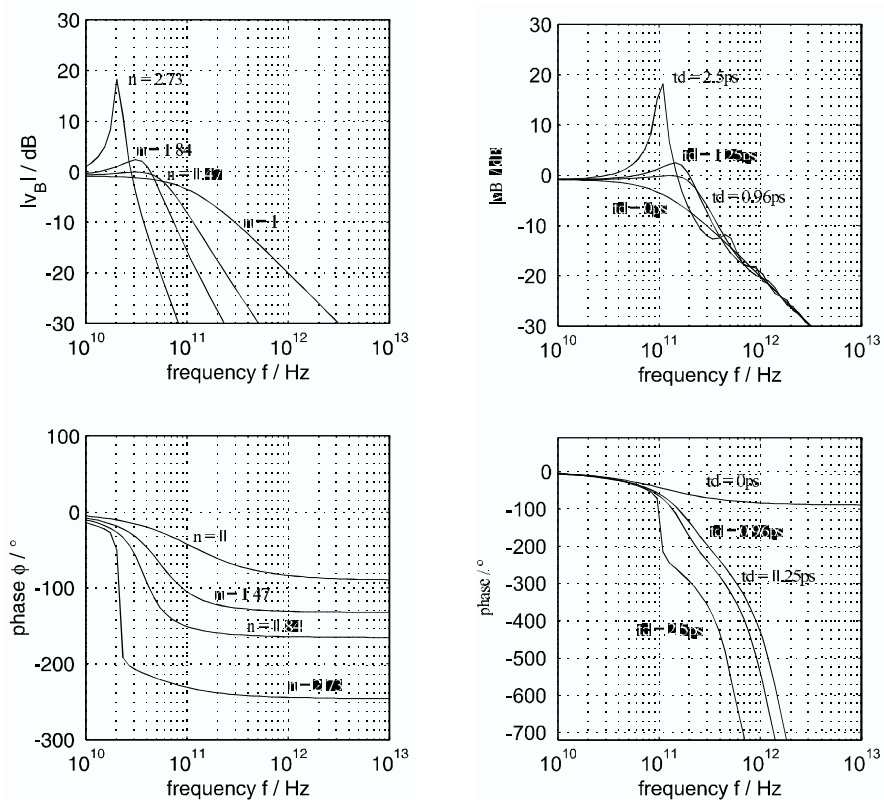
2. The Optimized Structure of Negative Feedback Amplifier

The best implemented amplifier has to be adapted to theoretical concepts as good as possible. The buffer amplifier (unity gain amplifier) as the current-to-voltage converter have severe problems because of their 100 % negative feedback. There are many discrepancies to the ideal concept, mainly in the region of medium frequencies: The transition region between low and high frequencies will mainly determined by the phase margin:

$\varphi \approx 90^\circ$	asymptotic transition
$\varphi_{Res,T} = 64.83^\circ$	aperiodic limit: Increase of amplification to $\|A\| = 1$
$0 < \varphi_{Res,T} < 64.83^\circ$	not acceptable peak in the transition function: $\|A\| \gg 1$;
$\varphi_{Res,T} \leq 0$	unstable amplifier, oscillator

3. Instability of the Unity Gain Amplifier

The problems of multiple poles (n) is well known in literature. In this treatment n should be a variable real number, that means a "variable phase shift" in the open-loop gain. In this case there is a good approximation of the open-loop gain with different cut-off frequencies near the critical transit frequency. Figure 2a shows the result of the variation of n in the case of the unity gain amplifier very impressive. The inner transistor amplification is $g_{i,DC} = 10$, and the cut-off frequency $f_o = 10$GHz.



(a) (b)

Fig. 2. Frequency response in the case of destabilisation by (a) multiple poles n, (b) delay times t_d

With $n = 1.47$ the increase of amplification to the desired value of 1 can be reached (aperiodic case). The enlargement of n results in a lower phase margin at the transit frequency of the open-loop gain.

The problems of delay times in circuit layout are undervalued in literature. The result is a lower phase margin at the transit frequency. An unavoidable pole in the open-loop gain will add a phase shift of 90° maximum. In the case of delay times phase shifting is unlimited without reducing the absolute value of the open-loop gain (which would improve the phase margin). Figure 2b shows the frequency response of the amplification under the influence of destabilisation by delay times.

It is possible to interpret the delay time as transit time over a geometrical length L. (Look at figure 3.) It depends on the velocity of the

electromagnetic waves. The formula is

$$L = vt_d$$

with $v = c/\sqrt{\mu_r \varepsilon_r}$, c is velocity of light and $\mu_r = 1$.

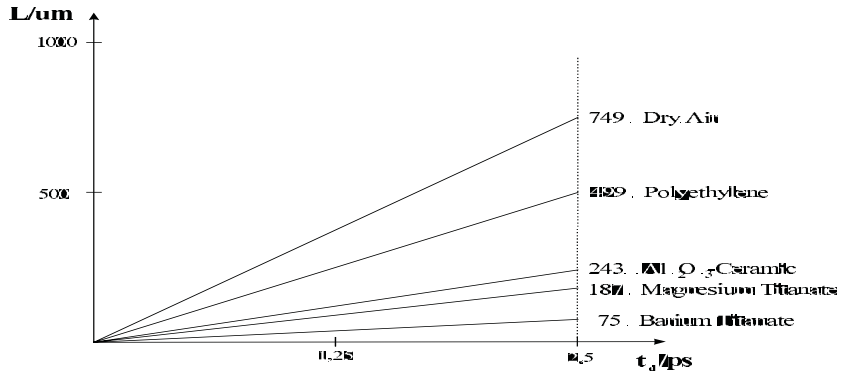


Fig. 3. Delay time caused by geometric length, different substrates

The consequence of these small geometric dimensions, all in the sub-millimeter range, is the implementation of the circuits in the technology of microelectronics. This is necessary even if the feedback is applied only to one stage just as emitter-follower or current-to-voltage converter. It is obvious that in the frequency range of 10 to 100GHz the boundaries of technology in microelectronics will be reached so that negative feedback is possible only in a moderate amount, that means lower than 100 % to improve the phase margin of the loop.

4. Moderate Negative Feedback in Ultra Fast Receivers

The regarded circuits in the last chapter have a feedback gain near -1. The negative feedback is about 100%. In this case, the influence of parasitic elements is dramatically large. The structure of these circuits prevents the reduction of feedback to a moderate value with more phase reserve, in principle. Therefore TISs and EFs are not suitable for ultra-high frequency applications. Negative feedback will be necessary in any case, of course. But the feedback gain should be chosen nearby zero at first. Then the increase of feedback gain will improve all specifications by the ratio of open-loop gain

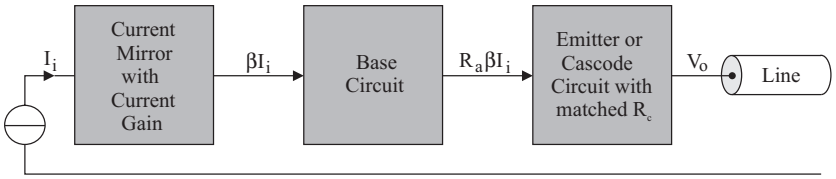


Fig. 4. Proposed transceiver circuit without TISs and Efs [6]

divided by closed-loop gain. But there is the risk of ringing and instability every time. Figure 4 shows the proposed transceiver circuit without TISs and EFs.

The detector current will be gained as much as possible by unsymmetrical current mirrors. The following simple base circuit has no negative feedback structure. Nevertheless, the cutoff frequency of the current-to-voltage conversion factor is near to the transition frequency of the current gain of the transistor. Last stage should be a stage which is suitable for matching the characteristic impedance of the connected lines as good as possible. The cascode circuit is the best one because it is suppressing the Miller effect very well.

In any case feedback structures have to be regarded with greatest attention. The given theoretical background helps to analyze the problem and to find a better solution. Optimal circuits have a tuning feedback struture to realize an aperiodic behaviour. The presented methods could be applied to all ultra-fast electronic circuits like amplifiers or buffers.

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