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A WIDE–BAND UNIFORM SAMPLING OF PERIODIC SIGNALS

Petar Bošnjakovic, Milica Dohčević–Jerotić and Darko Radjenović

Abstract. This paper describes a method for a uniform sampling of periodic signals based on using successive $f \to V$ and $V \to f$ conversion. It is shown that a conventional analogue–to–frequency converter is suitable to be used as a controllable pulse generator providing the sampling pulses the frequency of which is proportional to the sampled signal frequency. The proposed approach eliminates disadvantages of conventional methods: jitter inherent to implementation of phase–locked–loop and truncation error of programmable pulse–rate–divider. This allows implementation of the double–conversion method in high precision industrial and laboratory measurement instrumentation. The practical solution is described and the experimental results are also presented.

1. Introduction

Digital methods of processing has been widely used for the past two decades in digital instrumentation for the measurement of various periodic quantities. Uniform sampling strategy has been theoretically studied [1]–[4] and successfully implemented in many applications. A uniform sampling–time pulse generator (STPG), providing for M output pulses equally (regularly) spaced over the time interval consisting of the integer number N of the input signal periods, could be regarded as a frequency multiplier

$$f_s = kf_m, \tag{1}$$

where f_s is the sampling rate, f_m is the frequency of sampled signal and $k = M/N$ is the transfer constant.

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P. Bošnjaković is with Federal Buerau of Measures, Mike Alasa 14, 11000 Belgarde, Yugoslavia. M. Dohčević–Jerotić is with Belgrade Municipal Water Enterprise, Kneza Milosa 27, 11000 Belgrade, Yugoslavia. D. Radjenović is with Mihailo Pupin Institute, Volgina 15, 11000 Belgrade, Yugoslavia.

Operating principles of conventional uniform sampling–time pulse generators are based on programmable frequency divider (PFD) or phase–locked–loop (PLL). A sampling–time pulse generator (STPG) based on the programmable frequency divider method consists of an oscillator providing a pulse–train of a stable, reference frequency and a programmable counter–divider with a capacity proportional to the input signal period. It is a well known digital frequency multiplying technique which is used in communications, image processing, spectral analysis etc. The methods for noninteger frequency multiplication have also been developed [5]. In the precision measurements, the PFD method is primarily useful at relatively low sampling frequencies and as such has been implemented in microprocessor–based instrumentation with relatively low number of samples per sampled signal period [6]-[9]. Although the reference frequency does not appear in the transfer characteristic of the sampling generator, it determines the performance of the STPG. With either integer or fractional frequency multiplication, this method assumes that the instantaneous sampling period can take discrete values only since it is a multiple of a reference clock period. A finite resolution of sampling period means a truncation error in the determining of the sampling interval and non–uniform sampling as a result. Thus, a trade–off between the accuracy and the sampling rate has to be accepted. PLL method is a closed–loop method providing phase lock between the input signal and the feedback signal derived from the voltage–controlled oscillator (VCO) output signal through the appropriate pulse–rate divider [10]. The PLL systems (analog or digital) are widely used in communication, acoustics, control and measurement systems. In the steady state, the average value of the output pulse–rate is exactly equal to the input signal frequency multiplied by the division factor in the feedback loop. This property has been implemented for high resolution digital measurement of AC power frequency as well as for tachometers and automatic speed control od DC motor. In the field of fractional-N frequency synthesis more sophisticated techniques have been developed to provide noninteger frequency multiplication factor. A sampling frequency in order of tens MHz may be achieved using standard integrated PLL circuits. However, wide operating range, short response time and low output frequency jitter, caused by the residual ripple at the output of low-pass filter, are contradictory design requests, seriously limiting the performance of the basic PLL circuits when high precision measurements is to be considerd [11], [12]. When the loop filter is selected to provide high dynamic stability, the capture range becomes narrow and additional attention have to be paid to enable the PLL circuit to tracks the frequency of the input signal and to prevent the out–of–lock condition [13]. The lock–in state is to be monitored to ensure regular sampling [11], [14]. The change of

the sampled signal fundamental frequency from 50 Hz to 60 Hz requires an appropriate change of the filter parameters [11], [14]. The PLL lock range can be extended also by switching of the gain of the loop, by introducing automatic gain control for the phase detector output signal or by using an additional frequency discriminator [11]. But, these methods affect the VCO input and therefore the timing of sampling period. In the field of frequency synthesis more sophisticated, microprocessor based, techniques are developed to provide frequency multiplication factor which is not integer and to extend the lock range [15]. Generally, for high accuracy measurements of periodic quantities in power systems based on sampled data processing, this approach can be considered as satisfactory in the narrow frequency range only [11], [14], [16]. The objective of this paper is to present a new approach to the sampling–time pulse generator design based on the open–loop structure, providing high accuracy of multiplication factor and ensuring precision timing of output signal at high sampling rate. The proposed implementation of double conversion, from pulse to analog and backwards from analog to pulse, provide the linear transformation $f_m \rightarrow f_s$ in a wide range of input (sampled) signal frequencies without the truncation error and without the stability problems.

2. Operating principle of double–conversion sampling–time pulse generator

Linear transformation $f_m \rightarrow f_s$ can be performed using successive frequency–to–voltage and voltage–to–frequency conversion. Linear V/f converter having the transfer function

$$f = k_f V, \tag{2}$$

where V is input voltage and k_f converter transfer constant, is in fact a controllable pulse–generator, which could be used as a sampling–time pulse-generator. In order to satisfy relation (1), it is sufficient to apply, at the input of V/f converter, the voltage V proportional to the sampled signal frequency f_m

$$V = k_v f_m. \tag{3}$$

Generally, a condition to achieve desired linear conversion $f_m \rightarrow f_s$ is fulfilled if the $f \rightarrow V$ and $V \rightarrow f$ transformations are defined by a pair of inverse functions. As opposed to a PLL–based sampling–time pulse generator, this open-loop structure has no dynamic stability problem. Residual ripple at f/V converter output produces jitter, but it can be reduced to an arbitrarily specified level. This will reflect on the response time but without any

influence on the STPG stability or on the accuracy of the frequency multiplication. Precision measurements of periodic signals are primarily associated with measurements of electric quantities in AC power systems. Power network frequency deviates from its nominal value every time the power balance between generation and consumption is disturbed. As a quantity which is directly related to the energy stored in the power network, the line frequency is an inherently low rate–of–change variable. Therefore, fast response is not a requirement of the highest priority in a sampling–time pulse generator design.

2.1. Design

There are various commercially available integrated circuits capable to perform required conversions. Since the operating conditions for f/V and V/f conversion in an STPG are significantly different, the best cost-performance ratio has to be found. The input f/V converter operates at lower frequencies, consequently its high performance is easier to ensure. The performance of V/f is critical when a high sampling–rate is required. Therefore, a wide–range highly linear converter is necessary to implement. Using low–cost integrated V/f converters, such as $LM331$ and $VFC320$, the relative error less than 300 $\mu Hz/Hz$ can be obtained at input signal frequencies from 1 Hz to 100 Hz for $k = 2000$ [17]. The short-term stability of transfer constant of such an solution is in order of $\pm 20\, ppm/h$ and $\pm 50\, ppm/day$. The main source of error is the drift of 'zero' which is in order of $\pm 250\ \mu Hz/day$. In the range from 30 Hz to 80 Hz the relative nonlinearity error (maximum deviation of the $STPG$ input/output characteristics from a stright line drown through its end points) can be lower than 20 $\mu Hz/Hz$. Generally, the nonlinearity of the V/f converter is the dominant error source for high values of multiplication factor k. However, even for $k = 10000$ in the range ± 10 % of nominal power frequency the relative nonlinearity error is still lower than 200 $\mu Hz/Hz$.

3. High–performance double-conversion sampling–time pulse generator

Fig. 1 presents the proposed structure of the double-conversion sampling–time pulse generator offering a high accuracy in a wide range of input frequencies. Frequency–to–voltage conversion is performed using a pulse–wave–shaping: an input signal is transformed into the rectangular pulse train of the same frequency f_m , with constant amplitude V_R and constant pulse width T_1 . The average value V_a of such a pulse train is proportional

to the frequency f_m

$$V_a = T_1 V_R f_m. \tag{4}$$

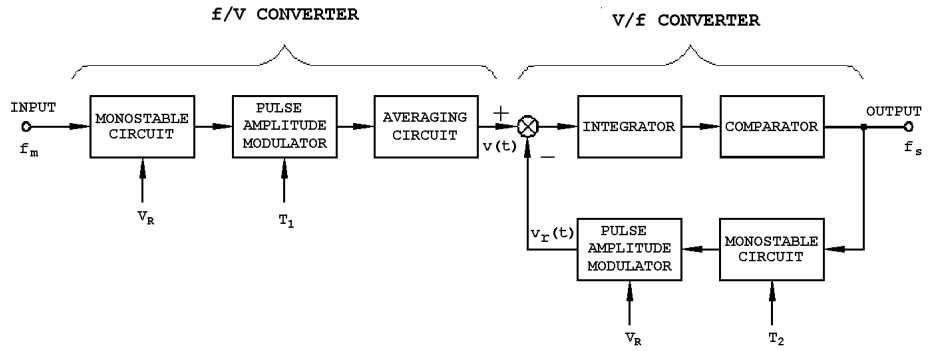

Fig. 1. Blok diagram the sampling-time pulse generator based on successive $f \to V$ and $V \to f$ conversion

The voltage–to–pulse–rate converter is a nonlinear feedback system composed of an integrator, comparator, monostable circuit and pulse–amplitude–modulator. A necessary condition to set this system in oscillating mode is that the input voltage is nonnegative and less than reference voltage V_R. A monostable circuit is triggered every time when the integrator output is increased above the predetermined constant level (comparator threshold). In the steady-state the balance is established between the input $v(t)$ and a feedback signal $v_r(t)$ which is a train of rectangular pulses with duration T_2 and amplitude V_R. The time interval between the two successive pulses, i.e. the period of oscillation T_s, is determined by an integral equation

$$\int_0^{T_s} [v(t) - v_r(t)]dt = 0. \tag{5}$$

As a consequence, the oscillation frequency f_S is given by

$$f_s = \frac{1}{T_2}\frac{V}{V_R}, \tag{6}$$

where V is the average value of the input voltage $v(t)$ during the time interval T_s

$$V = \frac{1}{T_s}\int_0^{T_s} v(t)dt. \tag{7}$$

The above structure may be considered as an inverse picture of the modulator–demodulator structure used for precision amplification of low–level analog signals. The goal of this paper is to show that new approach provides better performances than conventional methods for STPG design. The transfer constant of the system has no physical dimension. It is determined by the gain k_a (defined by a ratio of resistances) of the averaging circuit multiplied by the ratio of time intervals

$$k = k_a \frac{T_1}{T_2}. \tag{8}$$

Therefore, performance of this $STPG$ based on double-conversion does not depend on the reference voltage V_R which defines the amplitude of pulses. Moreover, since both of the time intervals T_1 and T_2 are defined digitally, e.g. in terms of referent clock period T_R

$$T_1 = N_1 T_R \qquad T_2 = N_2 T_R, \tag{9}$$

where N_1 and N_2 are integers, the transfer constant k is

$$k = k_a \frac{N_1}{N_2}. \tag{10}$$

It is independent of the clock period (assuming that only low–speed change i.e. drift exists) what ensures both high temperature and long–term stability of conversion. A sampling–time generator based on the proposed method was developed and tested. A slightly simplified schematic of custom designed circuit is shown in Fig. 2.

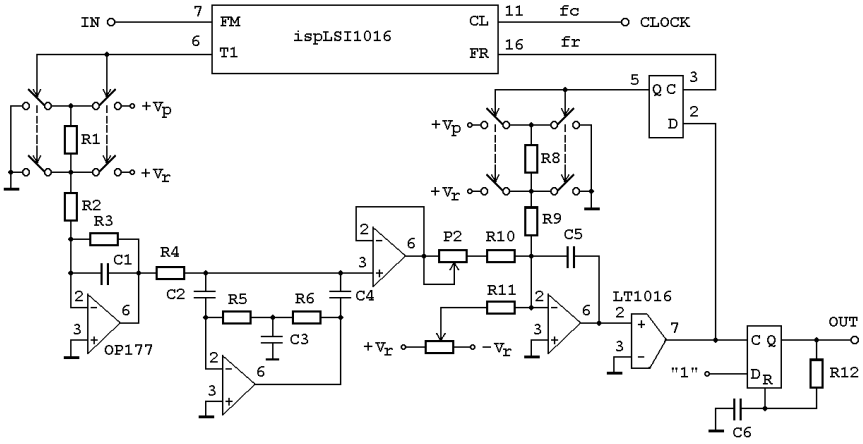

Fig. 2. A simplified schematic circuit of the double–conversion sampling–time pulse generator

The digital monostable circuit in the f/V converter is implemented by means of a presetable down counter. A special attention was paid to the design of the pulse amplitude modulator in order to minimize the effect of analog switch–on resistance on the transfer constant. A digital part of the generator was built using an in-system programmable complex logic device ($CPLD$) enabling computer control of the input and output frequency range. The output frequency relative error $\delta f_s/f_s$ of realized $STPG$ prototype for the input (sampled) signal frequency in the range from 20 Hz to 100 Hz is shown in Fig. 3. The gain drift is in order of ± 4 ppm/day. At 20 Hz input frequency, zero drift produces the output instability in order of ± 10 ppm/day.

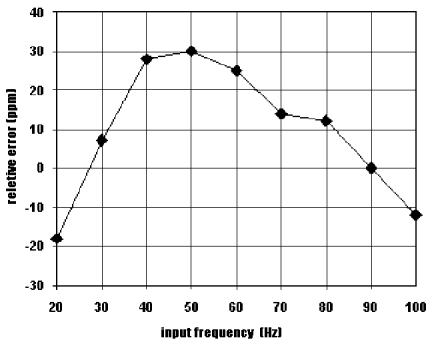

Fig. 3. The sampling–time pulse generator error

4. Conclusion

The paper proposes a double–conversion method for uniform sampling of periodic signals based on successive $f \rightarrow V$ and $V \rightarrow f$ transformation. This method provides high value of sampling frequency, high resolution of frequency multiplication factor, and wide-band operation without stability problems. Proposed structure provides a significantly wider input signal frequency range in comparison with the conventional PLL–based solutions of frequency multiplication problem.

The performance evaluation confirms the validity of described approach. Frequency multiplication by any real number (determined with the relative error obtainable with the implemented hardware) is allowed, when it is needed. The error lower than 20 $\mu Hz/Hz$ in the range 45 Hz to 66 Hz is achieved. For comparison, $STPG$ based on programmable pulse–rate–

divider providing similar performances should operate with the clock frequency in order of GHz.

The objective of this paper is to present a new approach to the sampling–time pulse generator design for high accuracy measurements of periodic quantities in power systems. The new design is based on the open–loop structure and offers equidistant sampling at high sampling rate.

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