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SYNCHRONIZATION OF DIGITAL COMMUNICATION NETWORK: TIMING SPECIFICATION, RECOVERY AND DISTRIBUTION

Grozdan Petrović, Ninko Radivojević and Radoslav Simić

Abstract. General timing model as well as specific characterization of timing information are discussed. Various techniques for extraction of the timing signal are analysed. In different phases of network digitalization possible solutions of reference timing information distribution are presented and discussed.

1. Introduction

The quality of services offered by digital communication network essentially depends on frequency accuracy and phase stability of synchronized clocks spread over different transmission and switching network elements. The goal of digital communication network synchronization is the implementation of reliable and high quality reference clocks and reliable and flexible distribution of reference timing information to all other clocks which have to be aligned with a reference timing signal. Such a synchronization distribution can be implemented by using three basic architectural models: plesiochronous, hierarchical masterslave and mutual [1,7,9].

There are many important factors concerning timing information distribution. Some of them depend of topology and organization of the whole network. The others depend on methods used for realization of basic network elements, transmission and switching equipment. If it is taken into account that existing networks are confronted with the growth of a number of customers and the growth of varieties of different integrated services, it

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Prof. dr G. Petrovic is with Faculty of Electrical Engineering, University of Belgrade, Bulevar revolucije 73, 11001 Belgrade, Yugoslavia, E-mail: epetrovg@ubbg.etf.bg.ac.yu. N. Radivojevic is with the Institute for Telecommunications and Electronics, IRITEL, Batajnicki put 23, 11080 Belgrade, Yugoslavia, E-mail: radni@iritel.bg.ac.yu. R. Simic is with Community of Yugoslav PTT–s, Palmotićeva 2, 11000 Belgrade, Yugoslavia, E-mail: rsimic@telekom.yu.

becomes evident that the synchronization problem is very complex. Due to these reasons, different subjects, scientific community, operators and standardization bodies invest a great effort to find the best and rational solutions for a number of important problems of theoretical, strategic, technical, administration and exploitation nature [1–33].

In this paper the view of relevant network synchronization problems is presented. The presentation is organised in the following way. In Section 2. the methods by which information of the timing signal is represented are discussed. Besides well known definitions, alternative criteria for representation of some phenomena are introduced. In Section 3. a review of various techniques for deriving the timing signal is presented. The solutions with the most employed circuit, a phase locked loop, are considered and some examples are given. Finally, in Section 4. the possible solutions of reference timing information distribution in different phases of network digitalization, as well as, with different multiplexing hierarchies (plesiochronous and synchronous), are proposed. The complete consideration is related to the model of hierarchical master-slave synchronization control method in typical situations for a country of medium size having an extensive development in telecommunications.

2. Timing specification

2.1 General timing model

Generally, timing in digital communication networks represents the rhythm by which data are collected, multiplexed, transmitted and switched. Timing information is an abstract description of timing on time and frequency scale.

Physically, timing information is carried by trains of pulses existing at the output ports of clocks or at the output ports of timing recovery circuits. These pulse trains are named timing signals, clock signals, or chronosignals.

For the purpose of the theoretical analysis and practical investigations, it is convenient to describe timing information using relatively simple models. Depending on the type of used signals (whether continuous or discrete) we can distinguish two models: continuos and discrete.

A. *Continuous model*

The continuous model is usually used in open literature. It is based on the concept that the timing signal (physical or logical) at any point within

network can be observed like symmetrically clipped frequency modulated sine wave. Analytically, such a timing signal is expressed as:

$$x_M(t) \equiv \mathrm{sgn}\left\{ A_M \sin\left[2\pi \int_{-\infty}^{t} (f_M + \nu_M(t))dt \right] \right\}, \tag{1}$$

where: A_M is the peak amplitude, f_M is a long–term mean frequency and $\nu_M(t)$ is the instantaneous frequency deviation. The instantaneous frequency deviation can be treated as the random time dependent process correlated with a number of other different processes specific for clock operation, multiplexing/demultiplexing mechanisms and propagation phenomena. For instance, some of these processes are: ageing, noise, power feeding instabilities and climatic conditions.

Substantially, the timing information of the timing signal $x_M(t)$ is represented by the argument of its sine wave function (see right side of Eq. (1)). This argument, known as *instantaneous phase*, can be written as:

$$\Phi_M(t) = 2\pi[f_M(t) + \varphi_M(t)] + \Phi_M(0) \tag{2}$$

where the component of the phase modulation is designated by $\varphi_M(t)$. $\Phi_M(0)$ is the initial value of the instantaneous phase for the selected reference instant $t = 0$. Comparing equations (1) and (2) it can be concluded that the following equation

$$\varphi_M(t) = \int_0^t \nu_M(u)du \tag{3}$$

stands. It is evident that $\varphi_M(t)$ can be, as well as $\nu_M(t)$, treated as time dependent random process. Generally, both processes, $\varphi_M(t)$ and $\nu_M(t)$, are composed as a sum of two parts from which one is "deterministic" and the other is noise like. Under "deterministic" part, a component, whose flow in time is entirely predictable when causing processes, is implied. On the other hand, in the case of noise part, the time flow of the process is not foreseeable.

In some ways, every timing signal determines its time scale. Accuracy with which it is attained can be estimated only in respect to the selected reference timing signal. Theoretically, we can imagine an ideal reference, i.e. the timing signal with the instantaneous phase $\Phi_I(t) = 2\pi f_I t + \Phi_M(0)$ where f_I denotes the nominal or desired frequency of the observed timing signal.

Then, time scale of the observed timing signal $x_M(t)$ can be represented by the *time signal*, $T_M(t)$, defined as:

$$T_M(t) = \frac{p_M(t)}{f_I} = \frac{f_M}{f_I}t + \frac{\varphi_M(t) + p_M(0)}{f_I}, \tag{4}$$

where: $p_M(t) = \Phi_M(t)/2\pi$ denotes a *normalized instantaneous phase.*

In reality, an ideal timing reference does not exist and we are addressed to the real reference with the time signal $T_R(t)$ having the form given by Eq. (4), but with components ($f_R, \varphi_R(t)$, and $p_R(0)$) which are, from the observer's point of view, known and well specified.

The error of time scale determination by the observed timing signal with respect to the selected reference is defined as:

$$TE_{MR}(t) = T_M(t) - T_R(t) \tag{5}$$

and is called time error. Very often it is convenient to present it in normalized form which can be provided dividing by reference timing signal period $1/f_R$. Then, the normalized time error $f_R TE_{MR}(t)$ is measured by *unit interval* (UI) of the selected reference timing signal. Having in mind, that the relative difference between f_R and f_I has to be extremely small, the important approximation

$$f_R TE_{MR}(t) \approx p_M(t) - p_R(t) \tag{6}$$

is obtained.

Together with the time signal, the time error represents an essential criterion for timing information specification by using continuous model.

B. *Discrete model*

Using discrete model timing information is represented by the counting process $Q_M(t)$, defined as:

$$Q_M(t) = i, \quad \text{for} \quad t_i^M \leq t \leq t_{i+1}^M, \tag{7}$$

where t_i^M denotes the epoch at which appears the i-th individual pulse of timing signal $x_M(t)$. The plots in Fig.1 illustrate the relation between $x_M(t)$ and $Q_M(t)$. Also the plot of $p_M(t)$ (supposing convenient justifying of $p_M(0)$ for the selected time reference $t = 0$) is shown. It is evident that $p_M(t)$ can be viewed as special smooth approximation of step–wise process $Q_M(t)$.

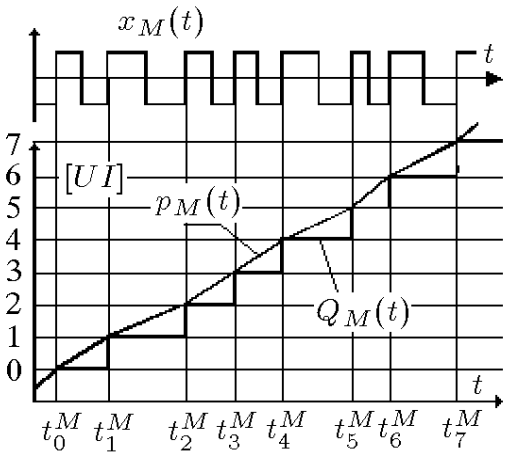


Figure 1. Illustration of signals used for timing specification purpose.

An important property of the counting process $Q_M(t)$ is that it can be directly evaluated by using simple counter device. Having in mind Eq. (6), this further suggests that the normalized time error $TE_{MR}(t)$ can be practically estimated as the difference of two counter contents, one counting observed timing pulse trains and the other counting reference timing pulse trains. The simplified block diagram of such time error estimator is shown in Fig. 2. The estimation period is bounded by neighboring reset events which occur when the content of reference counter reaches in advance prescribed level n.

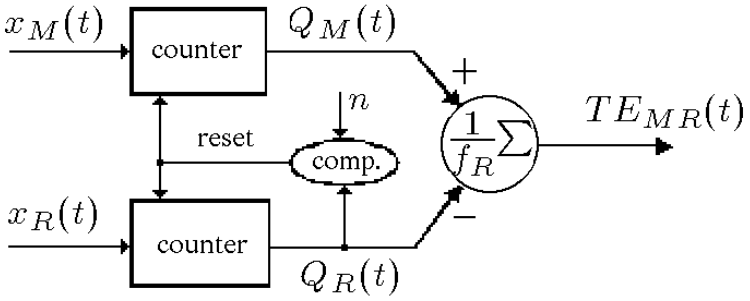


Figure 2. Schematic diagram of the time error estimation.

Using discrete model for timing information presentation we can also define the discrete–time instantaneous frequency

$$F_M(t) = \frac{1}{t_{i+1}^M - t_i^M}, \qquad \text{for} \qquad t_i^M \le t \le t_{i+1}^M \tag{8}$$

and corresponding discrete–time instantaneous normalized phase

$$P_M(t) = \int_{t_0}^{t} F_M(u)du = F_M(t)(t - t_i^M) + Q_M(t), \qquad t_i^M \le t \le t_{i+1}^M \tag{9}$$

From these definitions it can be shown that $P_M(t)$ is the linear–wise approximation of the both $p_M(t)$ and $Q_M(t)$. Based on theory of least–squares data smoothing, $F_M(t)$ and $P_M(t)$ can be used for precise formulation of long–mean frequency f_M and "deterministic" part of instantaneous frequency deviation $\nu_M(t)$. Also, signals $F_M(t)$ and $P_M(t)$ can be used for detailed time error analysis in multiplexing and demultiplexing procedures [34].

2.2 Specific timing characterization

A concrete characterization of timing information depends on whether the timing signal originates from an autonomous source, or it is derived by the timing recovery circuits. Autonomous sources in master–slave architecture represent primary references and classes of the slave references in the holdover or free running operation mode. On the other hand, timing recovery circuits, in a wide sense, represent a complete category of devices including very simple devices in the line regenerators, extractors in the receiving modules, various synchronization phase locked loops in multiplex and switching equipment and the variety of hierarchically organized slave clocks in normal operating conditions.

A. *Autonomous clock signals*

In the case of autonomous clocks, basic attention is paid to instantaneous frequency offset $\Delta\nu_{MR}(t)$ of the observed timing signal in relation to the "ideal" reference (i.e. the reference for which we can suppose $f_R = f_I$, and $\nu_R(t) = 0$). This criterion is defined by:

$$\Delta\nu_{MR}(t) = f_M + \nu_M(t) - f_R = f_R A_{MR}(t), \tag{10}$$

where with $A_{MR}(t)$ the instantaneous accuracy is designated. In the simplest, but from the practical point of view the most important case, $A_{MR}(t)$

can be represented like sum of three components: (i) deterministic long–term accuracy $a_{MR} = (f_M - f_R)/f_R$; (ii) deterministic linear with time growing drift $(f_M/f_R)D_M t$ (D_M is called *fractional linear drift coefficient* [7]); and (iii) a zero mean noise $\rho_{MR}(t)$. The power spectrum of noise component is characterized by sum of five parts, each of them proportional to the k-th power of frequency. These parts are called [7,14]: *Random Walk Frequency Modulation*, for $k = -2$; *Flicker Frequency Modulation*, for $k = -1$; *White Frequency Modulation*, for $k = 0$, *Flicker Phase Modulation*, for $k = 1$; and *White Phase Modulation*, for $k = 2$.

The problem with the instantaneous frequency offset $\Delta\nu_{MR}(t)$ and its components is that they can not be directly measured. In practice, these magnitudes are estimated on the basis of time error analysis. Basing on definition given by Eq. (5), we obtain:

$$TE_{MR}(t) \approx a_{MR}t + \frac{D_M t^2}{2} + \xi_{MR}(t), \tag{11}$$

where $\xi_{MR}(t)$ represents random component which depends on $\rho_M(t)$ and $p_M(0) - p_R(0)$.

But, although $TE_{MR}(t)$ can be measured, the problem is not completely solved because the difficulties of particular determination of parameters a_{MR}, D_M and $\xi_{MR}(t)$ remain. In essence, in theoretical papers and the existing standards there is a proposal of an indirect estimation of these parameters by statistical analysis of differently transformed $TE_{MR}(t)$, known as: *Time Interval Error* ($TIE(\tau, t)$), *Maximum Time Interval Error* ($MTIE(\tau, t)$), *Allian Time Interval Error* ($ATIE(\tau, t)$) and *Modified Allian Time interval Error* ($MATIE(n, \tau, t)$). Definitions, meaning and results of the carried analysis of these criteria are given in references [7] and [8]. Instead of repeating the details, in this paper only the schematic presentation of the mentioned criteria and analyzed statistical quantities as it is given in Fig.3 are discussed. Considering the possible effects of shown equivalent digital filtering it can be concluded that the result of the whole performed analysis is quite uncertain in distinguishing the contribution of particular instantaneous frequency offset components.

Additionally to the quantities based on time error analysis, there are a lot of supplement parameters (stability, temperature sensibility, working age, volume, weight, consumption, price etc.) characterizing autonomous clocks. The review of these parameters for a wide range of different clocks can be found in Ref. [19] and other papers of the Proceedings of the IEEE, appearing in July 1991.

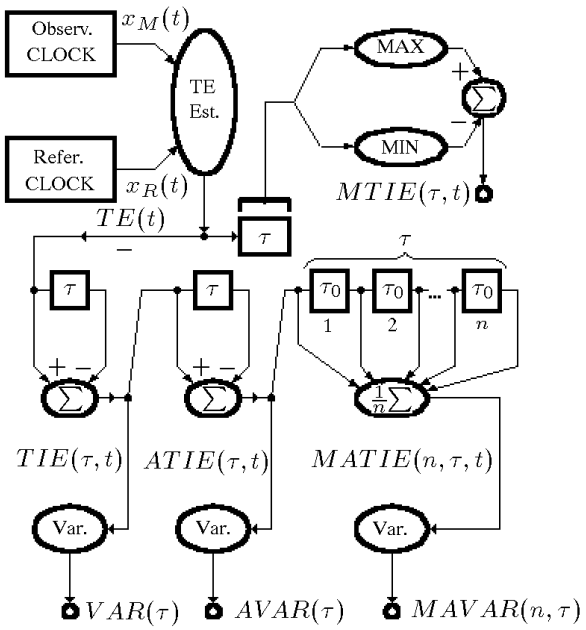


Figure 3. Schematic presentation of the time error analysis specific for autonomous clock signals.

B. Extracted clock signals

In specifications of timing signals derived by timing extractors the time error is also a basic criterion. It is specific in this case that the observed timing signal and the selected reference should have the common source clock as shown in Fig. 4. Therefore, it can be supposed that observed and reference timing signal has equal long term frequencies (i.e. $f_M = f_R$) and equal deterministic parts of its frequency deviations (i.e. $D_R = D_M$). So, starting from equation (5), it can be concluded that normalized $TE_{MR}(t)$ becomes proportional to the noise component $\xi_{MR}(t)$ introduced in subsection A.

The power and the spectral properties of the time error depend on network distribution facilities, primarily on implemented transmission systems. One of the objectives of the timing extractor design is to suppress the undesired contributions in the best fashion. On principle, this can be achieved on the satisfactory level only for the stationary (time invariant) part of the time error, known as jitter. Jitter degrades the quality of transmitted signal

by causing the effects of the phase modulation and by increasing the bit error on individual transmission links. On the other hand, nonstationary (time dependent) part of the time error, known as wander, can cause the appearance of slips (i.e. insertion or deletion of data in the receiving phase) and may be controlled by implementing elastic buffers in network nodes [12].

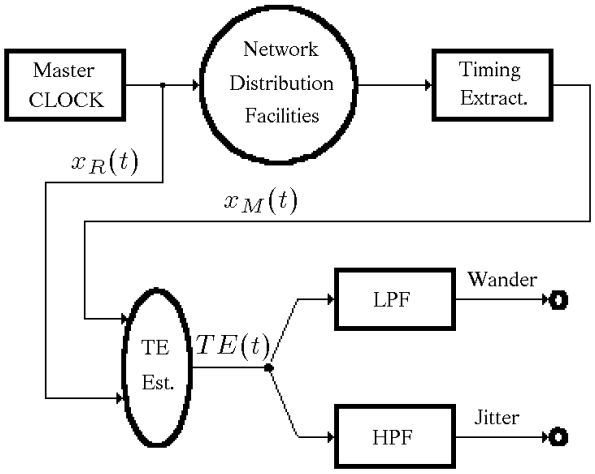


Figure 4. Schematic presentation of the time error analysis specific for extracted clock signals.

Decomposition of the timing error to jitter and wander is practically performed by complement low pass (LPF) and high pass (HPF) filters as shown in Fig. 4. The delineating frequency is standardized. The prescribed value depends on data rate, but in theoretical considerations frequency of 10 Hz can be accepted.

3. Timing recovery techniques

3.1 Introduction

The TRC (timing recovery circuit) is used in all digital receivers to recover (extract) a high quality clock signal (the optimum sampling clock signal) from the input random data stream. In PDH (Plesinchronous Digital Hierarchies) systems the timing recovery is mainly related with the optimum sampling clock signal for regeneration of input data. In SDH (Synchronous Digital Hierarchies) systems, besides the mention function, the timing recovery also serves in the first step for obtaining a high quality timing signal

in slave clocks.

The general block diagram of a timing recovery circuit is shown in Figure 5. The prefilter shapes the input signal s(t) to obtain the waveform as symmetrical as possible to improve the synchronization performance of the recovered clock signal (minimize jitter). A non–linear circuit is present when spectral line component at bit rate (f_0) is not available in received signal $x(t)$. If $x(t)$ is cyclostationary, with period T_0, a line component at $f_0 = 1/T_0$ (signal $c(t)$) can be extracted from signal $y(t)$ with bandpass filter [24,25].

All line codes used in digital transmission over metallic or fiber–optic cable belong to RZ (return–to–zero) or NRZ (nonreturn–to–zero) signals. RZ signal (usually 50% duty cycle) contains a line component at f_0, so nonlinear circuit is not needed. The examples of these codes are bipolar signals like HDB3, AMI etc. The NRZ signals mostly need nonlinear circuits such as: with square–low nonlinearity, a differentiator followed by a full–wave rectifier, EX–or gate to obtain a modified RZ signal. The bandpass filter passes the line component at a bit rate frequency and suppresses the adjacent continuous spectral components. LC tuned tank, SAW (surface acoustic wave) filter or PLL (phase–locked loop) are examples of a bandpass filter used in modern digital transmission systems. Owing to the possibility of monolithic integration, the PLL is the most frequently used method even at very high bit rates.

Figure 5. General block diagram of a timing recovery circuit.

3.2 PDH and SDH line systems

In PDH and SDH line equipment (line terminals, optical line terminals, line interface units, regenerators) the clock recovery circuit is a vital component. Parameters for PDH and SDH systems, which are the most important in designing timing recovery circuits: bit rate, line code for electrical and optical interfaces, minimum required bandwidth for jitter and maximum alignment jitter, are summarized in Table 1.

Digital multiplex, line and switching systems at electrical and optical interfaces have the following line codes: HDB3 (RZ bipolar, duty cycle 50%), CMI, MCMI (modified CMI) and ordinary NRZ (binary code). CMI and MCMI can be regarded as NRZ with a double bit rate ($2 * f_0$). The minimum

jitter bandwidth is a measure of TRC's ability to track a jittered input data. The alignment jitter, as a difference between input jitter and recovered clock jitter (displacement from the optimum time decision point), can cause errors in retimed data.

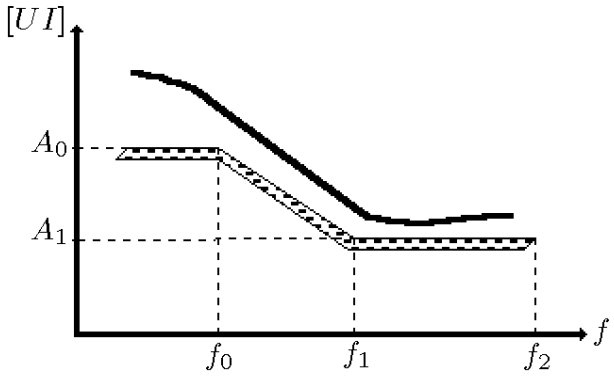
Example: For 155Mb/s (STM–1 level) ITU–T recommends in G.958 jitter transfer function (corner frequency is 130kHz for type A and 30kHz for type B regenerator, jitter peaking is 0.1dB) and jitter tolerance mask (type A: $f_0 = 6.5k$Hz, $f_1 = 65k$Hz, $A_0 = 1.5UI$, $A_1 = 0.15UI$; type B: $f_0 = 1.2k$Hz, $f_1 = 12k$Hz, $A_0 = 1.5UI$, $A_1 = 0.15UI$ referred to Figure 6)

Table 1. Parameters for PDH and SDH systems

ELECTRICAL INTERFACE				
BIT RATE Mb/s	Code	signal	Min bandwidth kHz	max alignment jitter U_{ipp}
PDH 2.048	HDB3	RZ(50%)	18	0.2
PDH 8.448	HDB3	RZ(50%)	3	0.2
PDH 34.368	HDB3	RZ(50%)	10	0.15
PDH 139.264	CMI	NRZ($2f_0$)	10	0.075
SDH 155.520	CMI	NRZ($2f_0$)	65	0.15 (0.075)
SDH 622.080	binary	NRZ	250	0.15
SDH 2 488.32	binary	NRZ	1 000	0.15

OPTICAL INTERFACE				
BIT RATE Mb/s	code	signal	min bandwidth type A type B kHz	max alignment jitter U_{Ipp}
PDH 2.048	MCMI	NRZ($2f_0$)	*	*
PDH 8.448	MCMI	NRZ($2f_0$)	*	*
PDH 34.368	MCMI	NRZ($2f_0$)	*	*
PDH 139.264	CMI	NRZ($2f_0$)	*	*
SDH 155.520	binary	NRZ	65 12	0.15
SDH 622.080	binary	NRZ	250 12	0.15
SDH 2 488.32	binary	NRZ	1000 12	0.15

*) Optical interface is not defined for PDH systems



$34Mb/s : f_0 = 400\text{Hz}, f_1 = 3k\text{Hz}, f_2 = 400k\text{Hz};$
$A_0 = 1.5, A_1 = 0.2;$

Figure 6. Measured maximum input jitter for OLT 34.

3.3 Phase–locked loops

A. *Acquisition and tracking mode*

The main parts of a PLL are: a PD (phase detector), a loop filter and a VCO (voltage controlled oscillator) [26]. The most popular in practice is the second order loop, with an integrator in the loop filter, which ensures no steady state phase error to remain. In timing recovery applications PLL has to be optimized in the following way. The choice of PD must take into account the effect of missing transitions. To keep the jitter within limits, the bandwidth of the PLL must be kept small but reliable frequency acquisition is only possible if the bandwidth is enough wide. To make a compromise between the acquisition and the tracking performances different techniques are known:

- dual bandwidth for acquisition and tracking mode [27],
- frequency sweeping the local VCO [26,28],
- employing a frequency tracking loop [29],
- use of a VCXO (voltage–controlled crystal oscillator),
- use of a reference (crystal controlled) clock [30]

PLL with VCXO is a common choice in many applications when the frequency tolerance of the input data is within frequency pulling range of the VCXO. The disadvantage of this method is expensive VCXO, very often with required large frequency pulling range to accommodate the specified input jitter.

Example: According to ITU–T Recommendation G.823 for 34Mb/s line systems the required minimum jitter bandwidth of PLL is 10kHz, so to accommodate sinusoidal input jitter, $I(t) = A_j \sin(2f_j t)$, with amplitude A_j and frequency f_j, minimum required pulling range of VCXO is:

$$\Delta f = \pm 2\pi \frac{f_j A_j}{2} = \pm 2\pi 10000 \frac{0.15}{2} = \pm 137 ppm.$$

Figure 6 shows measured jitter tolerance characteristic of optical line terminal operating at 34Mb/s (OLT) when the pulling range of VCXO is more than $\pm 300 ppm$.

B. *Jitter transfer function and jitter peaking effect*

The jitter transfer function is the ratio of the output and applied input jitter versus frequency. The maximum gain in the jitter transfer function (in dB) is called jitter peaking. It can contribute to the accumulation of jitter in a chain of regenerators. For a second order PLL the jitter transfer function is expressed as [26]:

$$H(s) = \frac{K(1+\tau s)}{(K + K\tau s + s^2)} \tag{12}$$

Due to the presence of the zero (for loop stability) at a frequency lower than that of the poles a jitter peaking occurs. This jitter peaking can be reduced by increasing the damping ratio but never completely eliminated. With increasing a damping ratio of the loop the acquisition speed decreases so the solution is not perfect. A better solution is to move the zero out of the forward path so that there is no closed–loop zero. This method is called Delay and Phase locked loop (D/PLL) and will be considered in subsection D.

C. *Frequency tracking loop*

The frequency tracking loop is based on an additional frequency detector (FD) in phase locked loop (Figure 7). The role of FD is to reduce a large initial VCO frequency offset to the small amount when PD takes over to complete the acquisition. The first FD, known as a quadricorrelator, was introduced in [31]. The digital implementation of the quadricorrelator, using a rotational frequency detector [32], has found application in many IC (integrated circuit) products for clock recovery. The advantage compared to the PLL with VCXO is that a simple VCO can be used. The disadvantage of this case is that the acquisition time can depend on data statistics and input jitter, also false locking is possible.

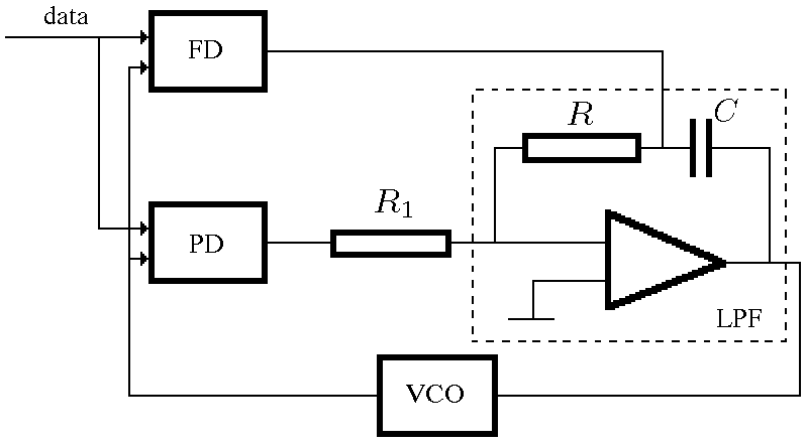


Figure 7. Frequency tracking loop – block diagram.

The fastest frequency acquisition occurs if the time constant of the acquisition is [32] :

$$T_{acq} = \frac{\tau 1}{K_0 K_d}, \tag{13}$$

i.e., if the FD directly charges the integrator capacitor (C in Figure 7). $\tau_1 = R_2 C$, K_0 is VCO gain constant, K_d is FD constant. Compared to this method some advantage is obtained by using a reference clock to keep the free running frequency of the VCO within lock–in range of the PLL, as proposed in [30].

D. *Timing recovery circuit for 155Mb/s (STM-1 level)*

Even at high bit rates the PLL has been the most popular TRC owing to the progress made in advanced techniques and monolithic integration. Today, many IC products are available in the market as TRC for 155Mb/s. Two methods implemented in IC are interesting: D/PLL [33] and digital quadricorrelator [35].

D/PLL eliminates jitter peaking effect owing to the principle shown in Figure 8. VCPS (voltage controlled phase shifter) and additional feedback path enable that the zero in the jitter transfer function, required to stabilize a second order PLL, does not appear in the closed–loop transfer function:

$$H(s) = \frac{K}{K + K\tau s + s^2} \tag{14}$$

Also, the required pulling range of VCXO, to accommodate the input jitter, is reduced due to the action of VCPS (flat portion in Figure 8). The same chip can be used in combination with SAW filter instead of VCXO.

With digital quadricorrelator (rotational FD) some advantages can be obtained: no external VCXO is required, VCO on the chip with stability better than 20%, in combination with advanced PD the pattern jitter is eliminated.

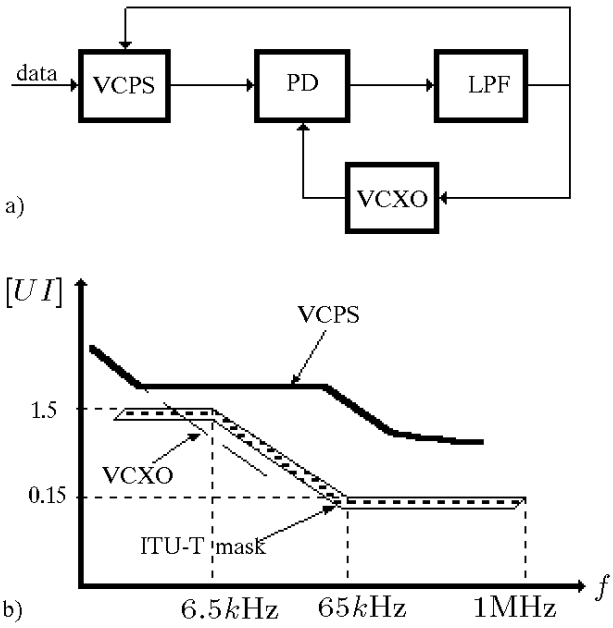


Figure 8. D/PLL basic principle: a) block diagram; b) jitter tolerance.

4. Timing distribution

4.1 General

In the integrated digital network (IDN) digital exchanges are interconnected with digital transmission systems. To avoid the loss of information, clocks of digital exchanges have to be synchronized or they must have proposed accuracy of their timing signals according to their ranges in the network. If digital exchanges are interconnected with PDH transmission systems synchronization problem is relating only to the switching systems and synchronous operation of their clocks. PDH transmission systems are

foreseen only for timing information distribution and realization of such synchronization network.

If digital exchanges are interconnected with SDH transmission systems problem of network synchronization becomes more complicated due to the fact that SDH transmission systems need synchronization as well.

On international links plesiochronous operation with frequency accuracy of reference clock better than 1×10^{-11} should be applied [22].

One or more synchronization methods, due to the network configuration, size of the country etc., is recommended. In the countries of the medium size hierarchical master–slave methods are recommended. Plesiochronous operation can be applied in the countries covering wide area or in the countries with a high number of international exchanges. In those cases, the areas of not less than one international exchange have to be synchronized and they must satisfy all conditions for national networks [22].

4.2 Network with PDH transmission systems

PDH transmission systems did not themselves require synchronization. Forming hierarchical digital signals of the higher order with bit rates greater than $2048k$bit/s is performing in digital multiplex equipment with multiplexing of tributary signals. Synchronization on higher bit rates is achieved by using justification methods [12].

The distribution of timing signals in PDH network has to be performed by using primary digital signals at $2048k$bit/s. Not all primary digital signals are used for transfer of timing informations but, when it is the case, the information about that is written in S_i bits ($i = 4, 5, 6, 7$ and 8) in the time slots 0 of frames not containing frame alignment signals [22].

When hierarchical methods are used for network synchronization the application of synchronization loops is not allowed. The applied method itself has to be very reliable which can be regulated through network synchronization plan with primary, secondary and etc. reference paths. Such paths should be the shortest, they should contain a minimum number of synchronization nodes and links and they should have maximum routing diversity.

4.3 Network with SDH transmission systems

SDH transmission systems are foreseen for synchronous or pseudosynchronous operation. Forming hierarchical digital signals in SDH is performed by using mapping, phase alignment and multiplexing [22]. It is known that positions of virtual containers VC–n in the STM–N frames ($N = 1, 4, 16, 64, \dots$) are determined with pointer values. When the timing signal of the incoming virtual container VC–n is not in compliance with

an internal timing signal of the STM–N multiplex equipment pointer will be activated. In that case VC–n frame is floating in the STM–N frame and its positions are determined through pointer values. The method of positive(zero)negative justification is used to synchronize timing signals of the virtual container VC–n and of the STM–N frame. This instability can be avoided if timing signals of virtual container VC–n and STM–N frame are synchronized or it can be brought to minimal amount if the mentioned timing signals are pseudosynchronous.

In this case for reference timing information distribution a method with hierarchical control has to be applied. It has the following levels:

- Primary reference clock – PRC (ITU–T Recommendation G.811)
- Slave clock in the transit node – SSU (ITU–T Recommendation G.812)
- Slave clock in the local node – SSU (ITU–T Recommendation G.812)
- Slave clock in the element of SDH network – SEC (ITU–T Recommendation G.813)

The PRC is the highest quality hierarchical clock and SEC is the lowest quality hierarchical clock. Higher quality clocks must not be synchronized from the lower quality clocks [23].

SSU (Synchronization Supply Unit) is located in every node of the synchronization network. It can be built in digital exchange, in element of the SDH network or it can be separated as an independent unit. The characteristics of SSU must be such that it is able to filter wander and jitter of the incoming digital signal and to separate information of the reference timing signal.

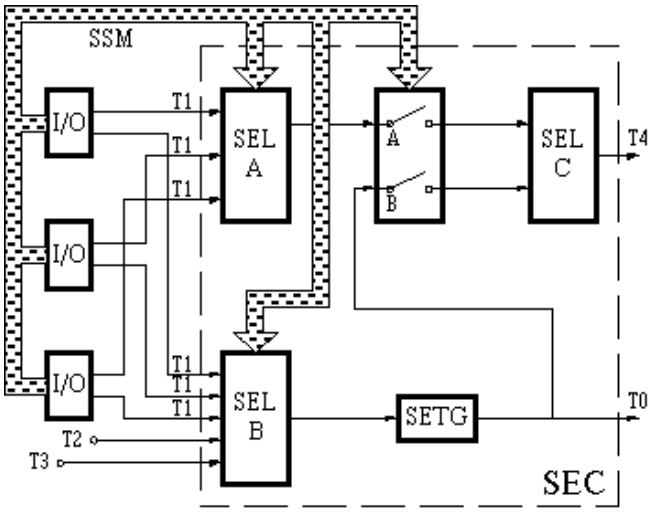
Elements of the SDH network (nodes of the SDH network not always coincide with nodes of the synchronization network) always contain SEC (SDH Equipment Clock), except in the case when they contain SSU.

The choice for extraction of the reference timing information in SEC is presented in Figure 7. It is important to point out that not all options from the same figure must be present in every SEC.

Switches A and B shown in figure 7 have very important role in forwarding reference timing information through nodes of the synchronization network as well as for avoiding the occurrences of synchronization loops [21].

The architecture of synchronization network realized with SDH transmission systems requires that all slave clocks (SSU and SEC) have to be controlled with reference timing frequency. Accordingly, the distribution of reference timing information has to be planned separately between all existing nodes of the synchronization network (internode–distribution) as well for every node of the synchronization network (intranode–distribution). In

the first case hierarchical control method has the same criteria as mentioned in subsection B. In the second case all slave clocks within any node derive information of the reference timing signal from SSU, which is traceable to the primary reference clock [22].



SETS– Synchronous Equipment Timing Source
SETG– Synchronous Equipment Timing Generator (PLL)
T0——Internal synchronization signals
T1——Sync reference derived from STM–N
T2——Sync reference derived from 2 Mbit/s
T3——2 MHz sync reference input
T4 ——2 MHz sync reference output
SEL—-Selector
SSM— Synchronization Status Message

Figure 9. Synchronization reference selection and timing distribution in SEC [21].

In the SDH networks reference timing information distribution is performed by using STM–N signals. Accordingly, in byte Z1 located in SOH (Section Overhead) of the STM–N frame, information of the quality of timing signal, which has to be derived from STM–N signal, is contained. That information, transferred by using bits 5, 6, 7 and 8 of the byte Z1, is called synchronization status message SSM. Every element of the SDH network which has more than one input of the STM–N signal will derive information about reference timing signal according to the level quality defined by SSM. In the case when SSMs have the same quality, priority has to be regulated through network synchronization plan of the IDN network.

4.4 Mixed PDH/SDH networks

In the transition period towards IDN network implemented only with SDH transmission systems a mixed PDH/SDH network will exist what will result in PDH islands and there will exist distribution problem of reference timing information through such mixed PDH/SDH network.

When the primary digital signal at $2048kbit/s$, intended to distribute reference timing information, is passed through SDH network it can be subject to the phase steps caused by pointer justification which may have a significant impairments to slaved clocks so it is not recommended to be used for synchronization. On the other hand, if aforementioned is not a case, due to the great flexibility of SDH network and potential rerouting of tributary primary digital signals through SDH network, it is complicated to differentiate which primary digital signal is suitable to carry information of reference timing signal through branchout transport network at $2048kbit/s$ level contained in SDH network.

This is another reason why distribution of reference timing signal at $2048kbit/s$ level is not recommended through SDH network and why it is necessary that STM–N signals carry timing information.

At the transitions points from PDH network to SDH network it is necessary to extract information of reference timing signal from incoming digital signal at $2048kbit/s$ and to insert it in STM–N signal. If there are other transition points from SDH to PDH network the inverse procedure is necessary and information of reference timing signal will be again in one primary digital signal at $2048kbit/s$ which is previously determined according to the network synchronization plan. In this way all aforementioned difficulties are removed and a very reliable distribution of reference timing information in mixed PDH/SDH networks is obtained.

4.5 Synchronization structures

Synchronization structures in dominantly SDH networks must guarantee that each element of SDH network and each switching system is traceable to primary reference clock, that no timing loop exists, and that synchronization can be restored in the case of single network failure.

In national networks the hierarchical control with spare synchronization paths is proposed to be used as the most commonly structure, see Figure 10. Good features of this structure are high reliability of synchronization network and a fact that synchronization loops are avoided.

In the ring and linear chain structures with the introduction of SSM byte, the restoration with reversal synchronization paths by ensuring that

no synchronization loops will be occurred is possible [20]. If the number of SECs in ring or linear chain structures is greater than 20, than intermediary SSU is required [22].

Star structures are applicable for intra–node distributions where SSU is used to synchronize a high number of the SDH equipment clocks.

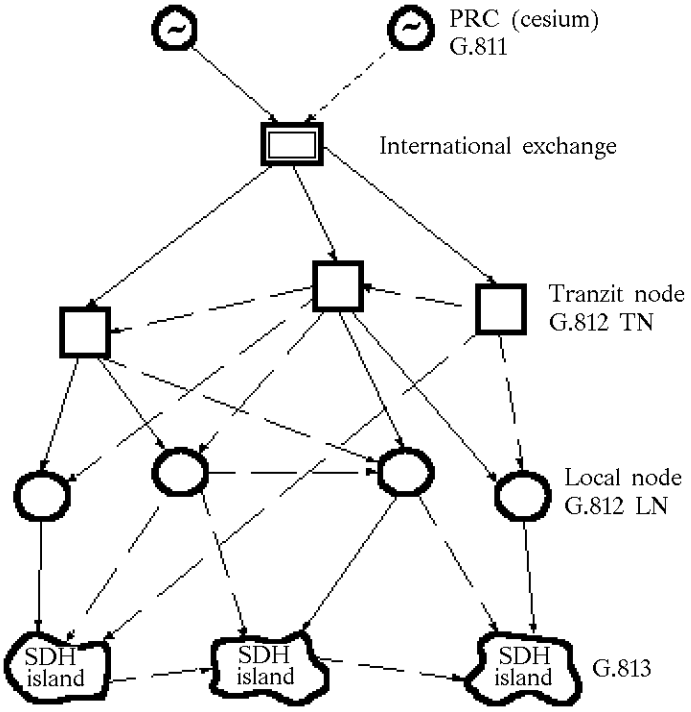


Figure 10. Hierarchical control structure.

Another new possibility is the use of the GPS (Global Position System) receivers for network synchronization which can provide qualities of timing clock better than 1×10^{-11}. In this case, reference timing signal can be used either as a standby or as an active reference. If it is used as an active reference the synchronization network is planned to work plesiochronously with a limited number of synchronous islands. The basic disadvantage of this method lies in the fact that it is controlled by the US Department of Defense.

Besides, GPS degradation occurs and often leads to synchronization problems. This can happen due to selective availability, interference from RF fields, weather conditions and many other factors. It is therefore essential to

include primary reference clock with cesium to ensure that network reference timing signal is in compliance with ITU recommendation G.811 at all times, even in the case of total loss or degradation of GPS reception.

5. Concluding remarks

Timing specifications, timing recovery and timing distribution are important topics concerning the digital network synchronization. In this paper, each of these topics was shortly enlightened having especial objective in mind. So, network timing was considered from theoretical standpoint and the objective was to discuss some known models relating to the time error and other timing criteria, as well as, to present some new ideas for further investigations. Timing recovery was considered from the standpoint of practical realizations. Review of techniques and solutions (based on employing various phase and frequency tracking loops) for extracting the timing information was presented. Finally, the instructions for reference timing information distribution in integrated digital networks implemented with PDH and SDH transmission systems was proposed. This was made in accordance with synchronization strategy currently being proposed by standardization organizations.

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