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SINGLE PHASE REVERSIBLE RECTIFIER WITH UNITY POWER FACTOR

Borislav Jeftenić, Milutin Petronijević and Nebojša Mitrović

Abstract. A detailed theoretical and experimental analysis of a single phase voltage sourced reversible rectifier (VSRR) with a unity power factor is presented in this paper. The complete model rectifier simulation in SPICE is used for the efficient work analyses. The special emphasis was given to analyses on the ripple effect of the DC output voltage and its asymmetry with respect to the neutral point. The influence of the controller parameters is analyzed on the mentioned effects. The prototype of described rectifier is realized and experimental results are shown. The simulation and experimental results show a good agreement and confirm a possibility of VSRR application to low power ranges.

1. Introduction

The latest international and national standards (IEC 555, JUS N.A6.101-103) define considerable rigorous conditions for a harmonic distortion and a minimum value of the power factor. The realization of the above mentioned standards has been being the research subject of the scientist in the field. Applications of novel components of power electronics make possible a flexible topology of the power converters and applications of new efficiency control techniques. The Pulse Width Modulation (PWM) with numerous variants is one of the possible direction in the solution of mentioned problems [1].The hysteresis control technique which was earlier known as an effective method of control in nonlinear systems also offers some significant advantages. The described technique makes the low noise operation possible.

A voltage sourced reversible rectifier (VSRR) with hysteresis control, near sinusoidal input current and unity power factor, and with a possibility of regulating DC busbar voltage, is analyzed in this paper. First of all, the

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Prof. dr B. Jeftenić is with University of Belgrade, Faculty of Electrical Engineering, Bulevar revolucije 73, 11000 Belgrade, Yugoslavia. B.S. M. Petronijević and M.S. N. Mitrović are with University of Niš, Faculty of Electronic Engineering, Beogradska 14, 18000 Niš, Yugoslavia.

principle of hysteresis control with the definition of the necessary conditions for its realization is described. On the basis of the system transfer function the appropriate PI control is chosen, after that the addition parameter adjustment is done by a computer simulation. The rectifier operation is simulated in the SPICE [11] program package. During the computer simulation, some of the problems were observed and their solution were required the modification of the control circuit.

A special attention is devoted to the problems of rectifier practical realization, and their solutions with a special review on the effects due to nonideal electronics components. The SPICE program package is used for a practical problem solution in a later phase of lab prototype making.

2. Description of the VSRR

2.1 Rectifier configuration and current forcing principle

The controlled single-phase rectifier configuration is shown schematically in Fig. 1. The switching elements $T+$ and $T-$ are power transistors (MOSFET) which maximum switching rate are about 10 kHz.

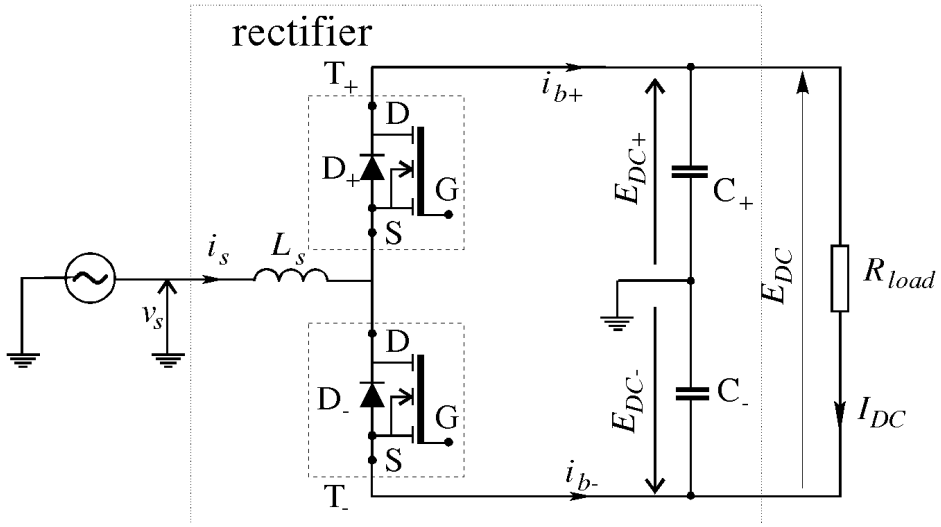

Figure 1. Single phase voltage sourced reversible rectifier.

The output capacitors (designated C_+ and C_-) have to charge up initially to the peak voltage of the utility supply, in order to controll the shown device

in a required manner. Realizing of the quote condition, which is one of the practical restriction of the proposed configuration, the principle of current forcing control can be realized. In Fig. 2., the line current i_s, reference current i_r, and voltage v_s of the rectifier input are presented.

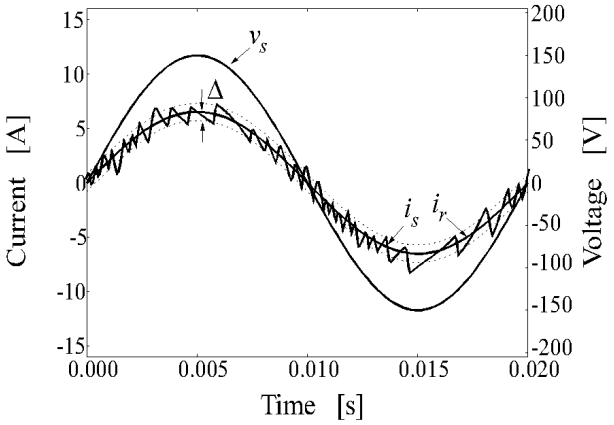

Figure 2. Simulated supply current bounded by hysteresis band.

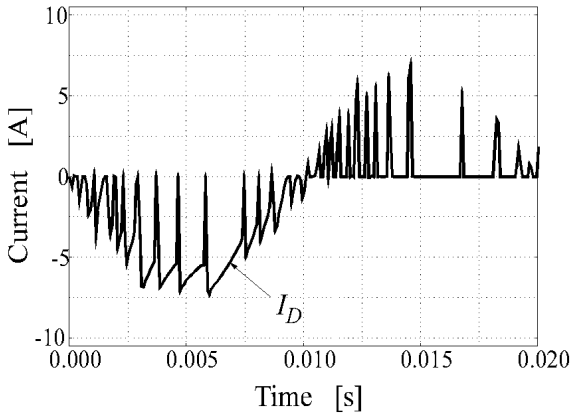

Figure 3. Simulated drain (I_D) current of the transistor T_+.

The capacitor C_+ is charged up by a diode D_+ in a positive semiperiode of the supply voltage. With increasing a voltage on the capacitor C_+, the supply current i_s decreases. When it is reached a value $i_s^* - \Delta$, a transistor T_- is turned on (where is i_s^* instantineous supply current reduce to controller level circuit and Δ hysteresis band). A current i_s increasing due to a sum

of voltage $v_s + E_{DC-}$. When i_s reaches a value $i_s^* + \Delta$, the transistor T_-, is turned off, a diode D_+ is forward bias ($v_s + L_s di_s/dt > E_{DC+}$) and over it the condenser C_+ is charged up again (L_s - supply inductance). For a negative semiperiode the description of rectifier work operations is similar. Simulated drain currents of the transistors T_+ and T_- are shown in Figs. 3-4. If the voltage drop of the inductor resistance and transistor on state voltage are neglected, the differential mathematical equation for the described converter are as follows:

$$pi_s = \frac{1}{L_s}(v_s - SE_{DC+} - (1-S)E_{DC-}) \tag{1}$$

$$pE_{DC+} = \frac{1}{C_0}\left(Si_s - \frac{E_{DC}}{R_{load}}\right) \tag{2}$$

$$pE_{DC-} = \frac{1}{C_0}\left((1-S)i_s + \frac{E_{DC}}{R_{load}}\right) \tag{3}$$

where $p = d/dt$ is a differential operator, $E_{DC} = E_{DC+} - E_{DC-}$, C_0 is a designed output capacitors value (realy $C_+ \approx C_0$ and $C_- \approx C_0$) and $S = 1$ if T_+ or D_+ is on, and $S = 0$ if T_- or D_- is on.

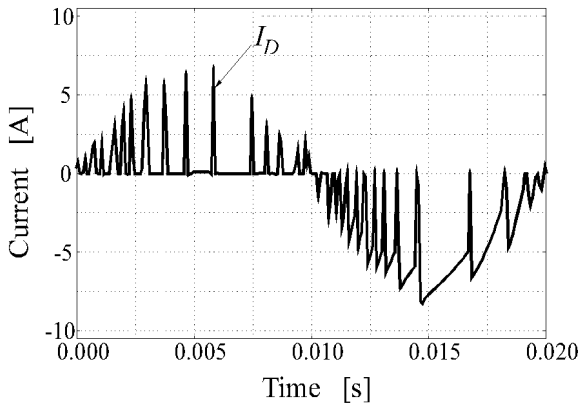

Figure 4. Simulated drain (I_D) current of the transistor T_-.

Using the equations (1)-(3) which describe power part of the rectifier and taking account a control strategy logic a VSRR can be simulated.

Consequently, the transistors and its inverse body diode appear as a bi–directional switch, the rectifier enables to operate with various power factor [3-4].

2.2 DC voltage control and power balance

The described rectifier has a possibility of voltage control in a definite voltage range. If the voltage drop is neglected, the minimum DC voltage is approximately equal to the double magnitude of the input AC voltage. The maximum of the output voltage is limited by the voltage capability of the switching components.

Assuming 100% efficiency and neglecting the DC busbar–voltage ripple, the power balance equation relating the AC power to the DC power can be written as [2]:

$$V_s I_s = \frac{1}{4} C_0 p E_{DC}^2 + \frac{E_{DC}^2}{R_{load}} \tag{4}$$

where is: V_s - RMS value of v_s, I_s - RMS value of the fundamental component of the i_s and E_{DC} - mean value of the total DC busbar voltage

It can be concluded that in a steady state, for the some load, the input rectifier current is risen with increasing the output DC voltage.

For the DC output voltage control the used control strategy is shown in Fig. 5. The control system has two regulators: master–voltage regulator, performed as the PI controller and slave–current regulator, performed as the hysteresis controller. The input of the PI controller is voltage error e, and the output is proportional to the required current for the reference DC voltage holding. To produce the necessary input rectifier current magnitude and near sinusoidal waveform, for the unity power factor operation, the output of the controller u^* is multiplied by the reduced AC supply voltage signal v_s^*. This signal is a reference input current i_r^* which is compared with an actual input current i_s^* in the hysteresis controller

For an adequate parameter tuning it is necessary to obtain corresponding transfer function $G_{rec}(p)$ ([2]).

$$G_{rec}(p) = \frac{E_{DC}(p)}{I_s(p)} = \frac{K_s}{p + \dfrac{2}{R_{load} C_0}} \tag{5}$$

where: $K_s = 2V_s / C_0 E_{DCr}$, and E_{DCr} is reference DC busbar voltage.

Consequently, the rectifier is the first order system. The parameters of PI controller are fitted on the basis of technical requirement (rise time and overshoot value) in the first step, and then because of the system nonlinearity, the fine tuning is made with a great precision using the model and experiment.

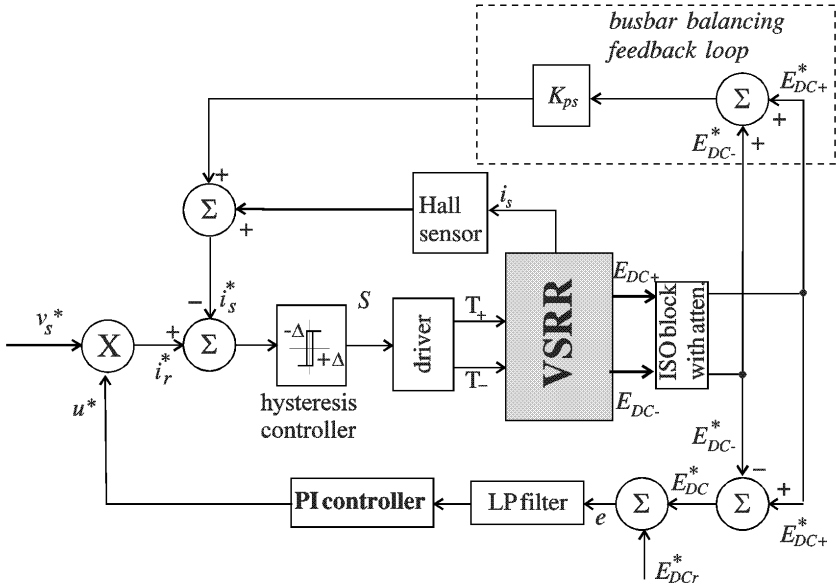

Figure 5. Hysteresis current–forcing controller.

2.3 DC busbar voltage ripple

The output signal of the PI controller is described by:

$$u(t) = K_p e(t) + K_i \int_0^t e(\xi) d\xi \tag{6}$$

where $e(t) = E^*_{DCr} - (E^*_{DC} + e^*_{AC}(t))$ is the error signal, K_p and K_i are proportional and integral gains, e^*_{AC} is the AC component of E_{DC}, and it is given by [2]:

$$e^*_{AC} = -\frac{I^*_{DC}}{\omega C_0 \sin(2\omega t)}. \tag{7}$$

The symbol * indicates the reduced quantities to the control logic level.

Substituting eqn. (7) into eqn. (6) gives:

$$\begin{aligned} u(t) = {} & K_p[E^*_{DCr} - E^*_{DC}] + \frac{K_p I^*_{DC}}{\omega C_0} \sin(2\omega t) + K_i[E^*_{DCr} - E^*_{DC}]t \\ & - \frac{K_i I^*_{DC}}{2\omega^2 C_0} \cos(2\omega t) + \frac{K_i I^*_{DC}}{2\omega^2 C_0}. \end{aligned} \tag{8}$$

In order to obtain the sinusoidal reference current, it is necessary that all parts be zero which contain second order harmonic, in the eqn. (8). The second member in the right side of the eqn. (8) is dominant in relation to the AC component which contains the coefficient K_i (the fourth member in the eqn. 8). To speed up the response time the increasing controller gain K_p is necessary. It will cause, at the same, time the effects reference and the supply current distortion. A compromise solution is done by using active lowpass (LP) filter which eliminates the 100 Hz frequency component, but at the same time slows down a dynamically response of the whole system. In this paper, the described compromise solution is used. The amplitude and phase characteristics of the applied low pass filter are shown in Fig. 6.

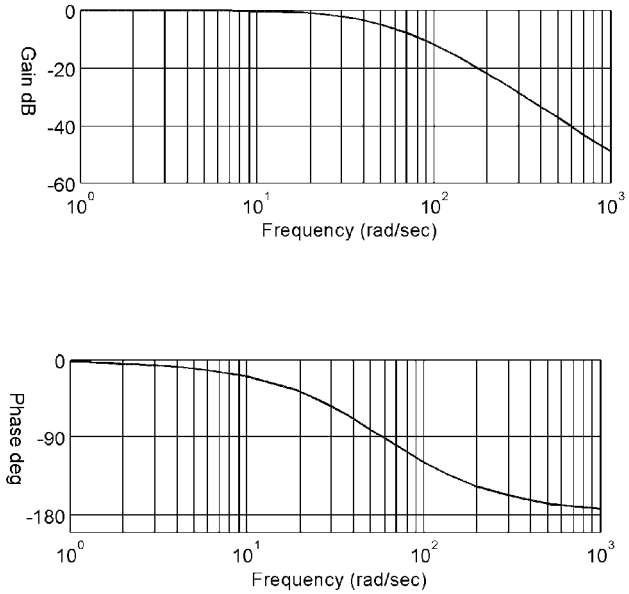

Figure 6. Amplitude and phase frequency characteristic of the applied LP filter.

3. VSRR design

3.1 Practical realization problems

During the practical realization of the whole device, several of the problems can appear:

- *The current limit of the transistor.* In order to rectifier overload protect, the output of the voltage controller must be limited according to the

maximum transistor current limit. The large size of C_0 also demands some kind of soft start that must be included during the initial charge up in order to prevent transient overshoot current which can damage of circuit components.

- *Ripple DC busbar voltage.* Since DC–side capacitance C_0 is a final value and each half of it is charged essentially on alternate half cycles of the input voltage waveform, the voltage ripple is present. This effect causes a reference current distortion. Tuning the controller and lowpass filter parameters has significtant effects on increasing or decreasing this effect.
- *DC busbar voltage asymmetry.* One reason of the unbalanced busbar voltage with respect to the neutral point, which can be expected in practical realizations, is the DC offset in the analogue multiplier. It can be eliminated by adding the passive filter which cut off the DC component of the signal reference current i_r. The second reason of the unbalance output voltage is the eventually non–equal DC busbar capacitance value. The effects can be eliminated by choosing adequately the DC side capacitances and including a busbar balancing feedback loop by summing E_{DC+} and E_{DC-} [1].

The previous list does not gather all problems which can be present during a practical realization of the VSRR (for example an overvoltage transistor protection, tuning drivers of circuit, etc.).

The simulation of VSRR in SPICE [11] program package is used, in order to avoid the experimental parameters tuning of the filter and the PI controller, having in mind the fact that the component can be damaged by an eventually error,

3.2 SPICE model VSRR and simulation results

In the SPICE model, which is used for the rectifier synthesis, the switching transistors T_+ and T_- are modeled by using the IRF840 library model. Every switch contains an appropriate RCD snubber circuit. The supply inductance and output condensers ($C+$ and $C-$) are modeled as ideal components. The control circuit is realized by using the library model of the operational amplifiers which are used later in the practical realization. Drivers' circuit is modeled as in [9]. In this manner it is taking account about the great number of the essential effects which are important for hardware implementations. The simulation model and whole system make the many-sided analysis of the components and the whole system possible.

The problems mentioned above are analyzed step by step by simulating on the described rectifier model. First, the output condensers were charged up by increasing gradually the supply voltage value. At the moment when it is

$t = 0.1s$ the hystreresis control is turned on. It is simulated a permanent DC offset reference current signal i_r^* from only $0.1A$, without an additional DC busbar balancing feedback. It can be observed that the DC busbar voltage does not differ from a reference value ($V_{ref} = 330\ V$), but output condensers voltage differ remarkably (Fig. 7.). The supply current obtained by the computer simulation is shown in Fig. 8. In some interval the supply current distortion can be observed, because of a permanent body diode forward bias.

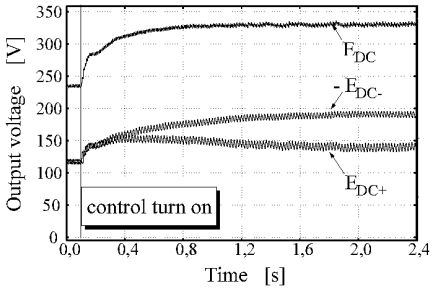

Figure 7. DC output voltage for the case of DC offset

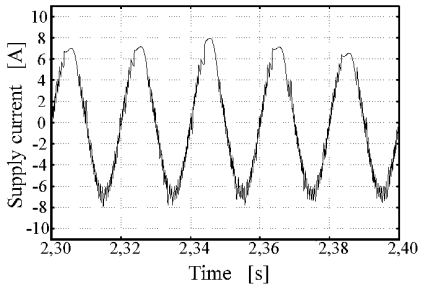

Figure 8. Supply current for the case of DC offset.

The non–equal DC busbar capacitance values make the DC busbar voltage to become unbalanced. Characteristic results (without busbar balancing feedback loop) are shown in Figs. 9 and 10.

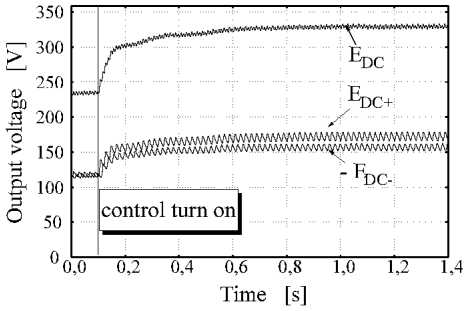

Figure 9. DC output voltage for the case non–equal output condenser.

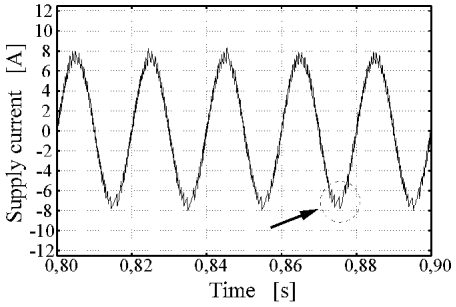

Figure 10. Supply current for the case non–equal output condenser.

Including the busbar balancing loop, the unbalance output voltage caused by the i_r^* current offset or by non–equal DC busbar capacitance value, is solved effectively. The obtained results are shown in Figs. 11 and 12.

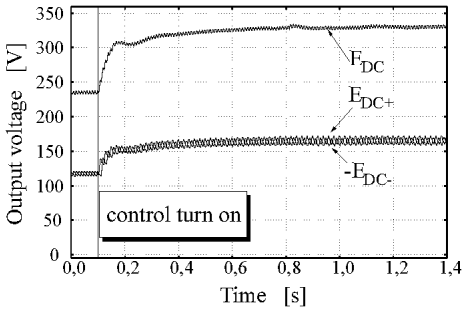

Figure 11. DC output voltage with busbar balancing loop.

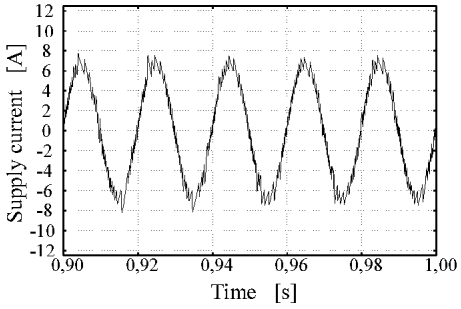

Figure 12. Supply current with busbar balancing loop.

In the no–load case ($R_{load} \to \infty$) the DC busbar voltage is without ripple (see the eqn. 9). The output DC voltage and supply current are shown in Fig. 13 and 14.

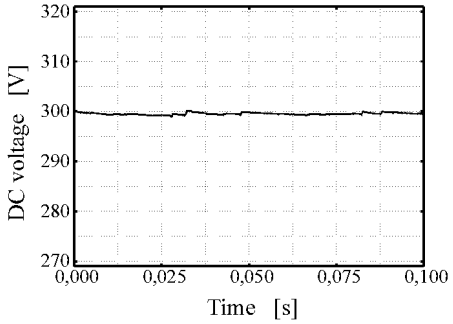

Figure 13. DC output voltage for the no–load case.

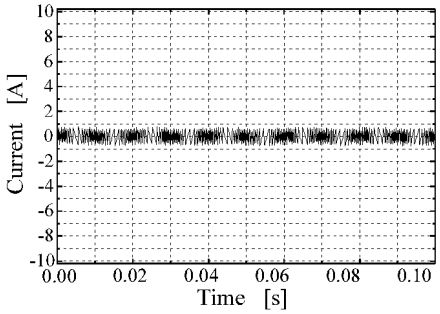

Figure 14. Supply current for the no–load case.

The other results will be shown by comparing with experimental results in the section 3.3.

3.3 Prototype realization and experimental results

On the basis of the research by a computer model, the laboratory prototype of the described rectifier is realized in the Electric Drives Laboratory of the Faculty of Electronic Engineering in Niš. Because of using MOSFET IRF840 (as switching transistor), the AC supply voltage is reduced to $110V_{rms}$. The rectifier control circuit is realized with an analogue technique

(driver circuit: IR2110, multiplier: MC1595, hysteresis controller and PI controller are realized by TL071/MC). The current is measured by a Hall's sensor. For an adequate tuning of the laboratory prototype, PI controller parameter optimization, as well as the low pass filter and the busbar feedback loop gain and so on, the characteristics results are recorded in different cases and compare. Because of the digital signal recording with low resolution, the shown signals are not fully reliable.

In Fig. 15 the supply voltage and current are shown. It can be seen that the zero displacement between voltage and current is obtained. The distortion of AC voltage supply is a voltage supply reduction consequence (the transformer saturation). A frequency spectrum of the line current is presented in Fig. 16. Clearly, the near unity power factor is reached. From Fig. 15 acording definition acepted in [3] the mean switching frequency can be estimate about 1 kHz.

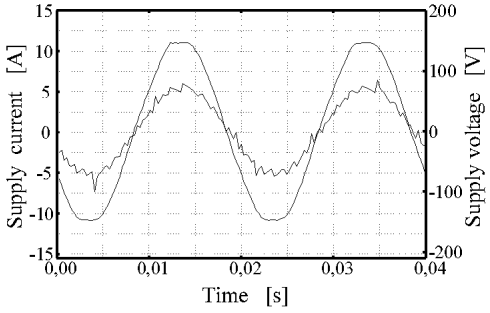

Figure 15. Supply voltage and current (experiment).

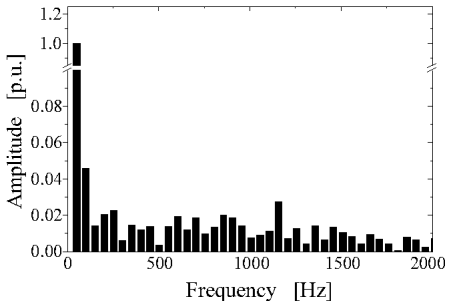

Figure 16. Line current harmonics spectrum (experiment).

The current forcing principle of the AC supply current is shown in Fig. 17. The presented signals are at the inputs of hysteresis controller. The DC busbar voltage is shown in Fig. 18. It can be seen that the DC output voltage ripple exists.

By decreasing the hysteresis band for the 50%, the maximum transistor switching frequency is increased about 50%. The AC supply current waveform for this case is shown in Fig. 19, and an appropriate frequency spectrum is shown in Fig. 20. The low harmonic specter distortion of the current can be seen. Undesirable effects are presented as increasing transistor switching losses.

Increasing of the switching frequency at the same inductance value (L_s), can be achieved by decreasing hysteresis band up to the value determined by practical limitations of the MOSFET IRF840 (switching losses, transistor maximum switching frequency and snubber design [3])

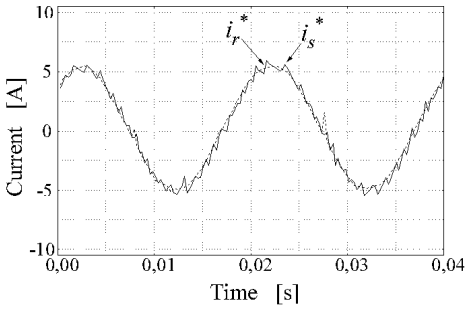

Figure 17. Supply i_s^* and reference i_r^* current (experiment).

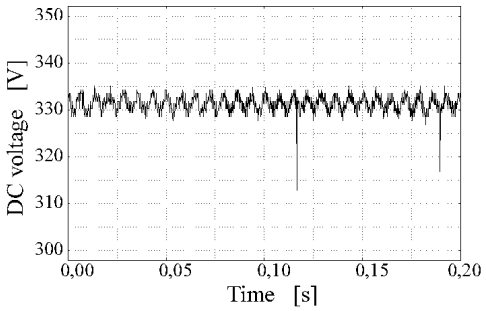

Figure 18. DC busbar voltage E_{DC} (experiment).

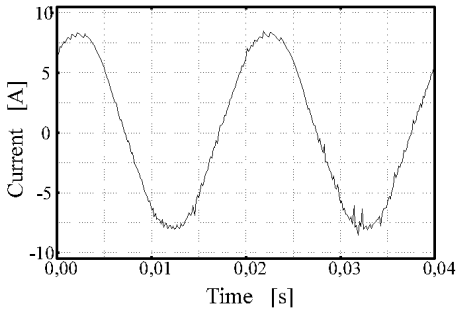

Figure 19. Supply current at decrease hysteresis band (experiment).

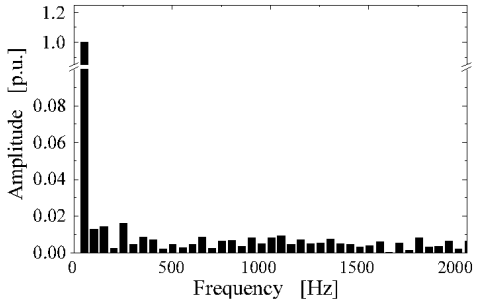

Figure 20. Supply current harmonic spectrum from Fig. 19. (experiment).

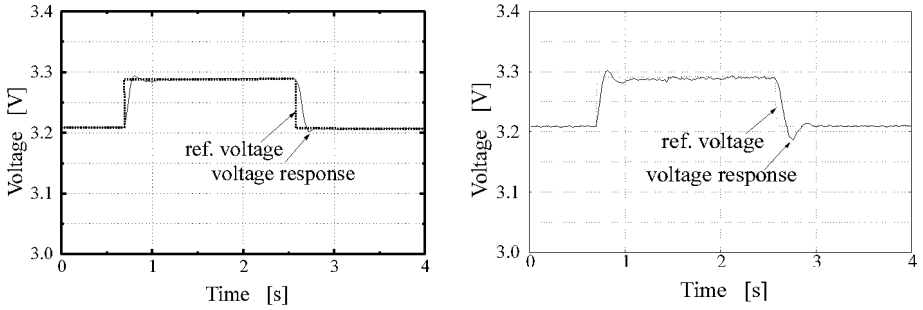

Figure 21. System response on step reference input a) (simulation) b) (experiment).

The important rectifier characteristic is the possibility of the DC busbar voltage control with a change of the voltage reference. The step response of E^*_{DC} obtained by the simulation and the experiment is shown in the Figs. 21a and 21b.

System response on load changes is illustrated on the Figs. 22a-22b.

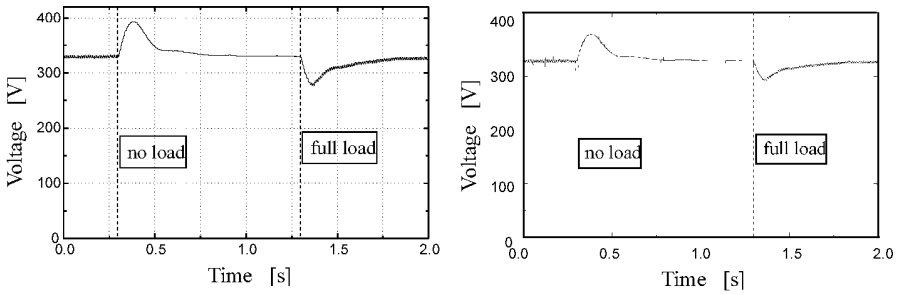

Figure 22. System response on load changes a) (simulation) b) (experimental).

For the $R_{load} = 220\ \Omega$ simulation and experimental results will be shown parallely. The characteristic results obtained by the computer model and by the experiment are presented in the Figs. 23-26.

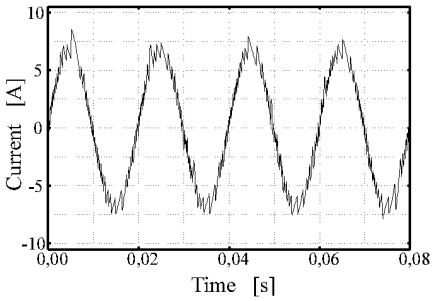

Figure 23. Supply current (simulation).

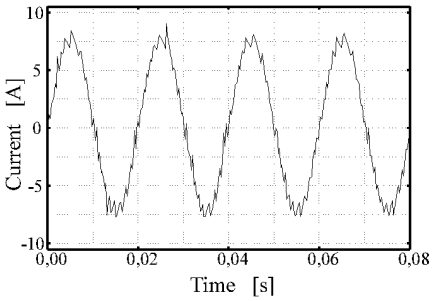

Figure 24. Supply current (experiment).

The possibility of the reversible operation was investigated with a computer model. The rectifier load is presented as the serial connection of the resistance and electromotive force E_{ems} with the variable magnitude. In the cases when electromotive force E_{ems} is greater than the reference voltage E_{DCref} the power will be back to the AC power supply.

The typical simulation results are shown in Fig. 27. and 28.

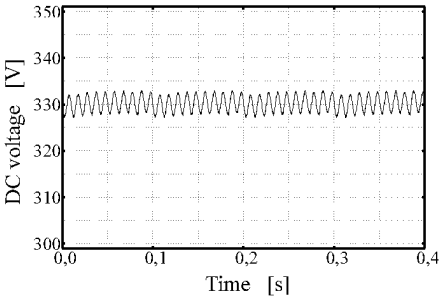

Figure 25. DC busbar voltage (simulation).

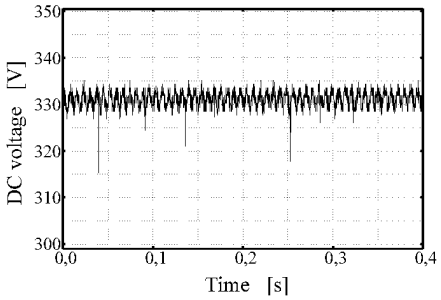

Figure 26. DC busbar voltage (experiment).

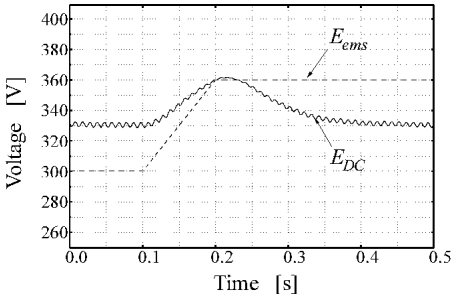

Figure 27. DC busbar voltage during the increasing of load electromotive force.

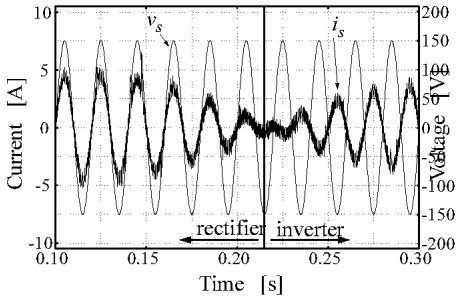

Figure 28. Supply voltage and current during the operating regime change.

4. Conclusion

The application of the rectifier with the unity power factor, especially in the low and middle power range, became very attractive due to a commercial availability of quality switching components of the needed current and voltage range. In this paper a phenomenology of the device is analyzed by the computer simulation and the experiment The advantage of the SPICE simulation is a possibility of researching device operation under conditions which are near to the reality (because of applying a reliable component model).

On the basis of the executed research the following solutions are proposed:

- The simulation and experimental results confirm the necessity of the filtering error signal to avoid the unwanted distortion of the reference current. In that manner the transient performance is degraded.
- On the basis of the simulation research, the optimal capacitance value of the output condenser for the limited ripple voltage is established.

- The influence of the DC offset in the controller analogue components can be reduced significantly by including a simple low–pass filter in the control loop and by adding the busbar balancing feedback loop.
- The other reason for the balancing feedback loop is the nonequality of the output condenser, although the influence is very small to the eventually voltage asymmetry.

The realized VSRR with the current–forced control make a good voltage regulation, sinusoidal line current and near unity power factor possible. The VSRR is very simple for the implementation, because a small number of the devices (only two MOSFET's). The device is suitable as a power source in variable speed drive systems with bi–directional power–flow capability.

The application of the realized prototype and single and three phase bridge rectifier configuration in the variable speed drive application will be considered in future papers.

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